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Analog Integrated Filters

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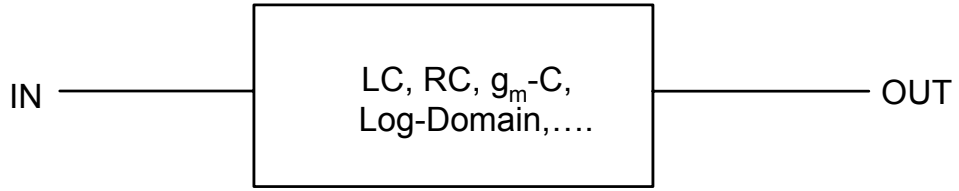
Part-I: Overview

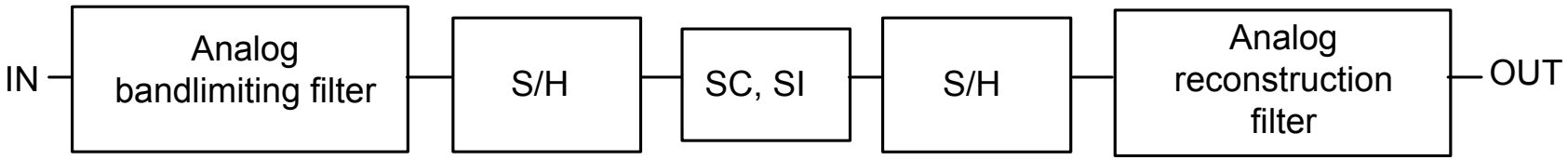
Classification of filters

– **Analog filters**

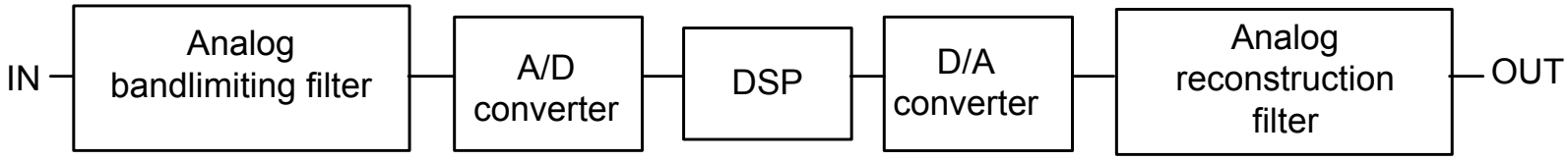
- Continuous-time



- Sampled-data



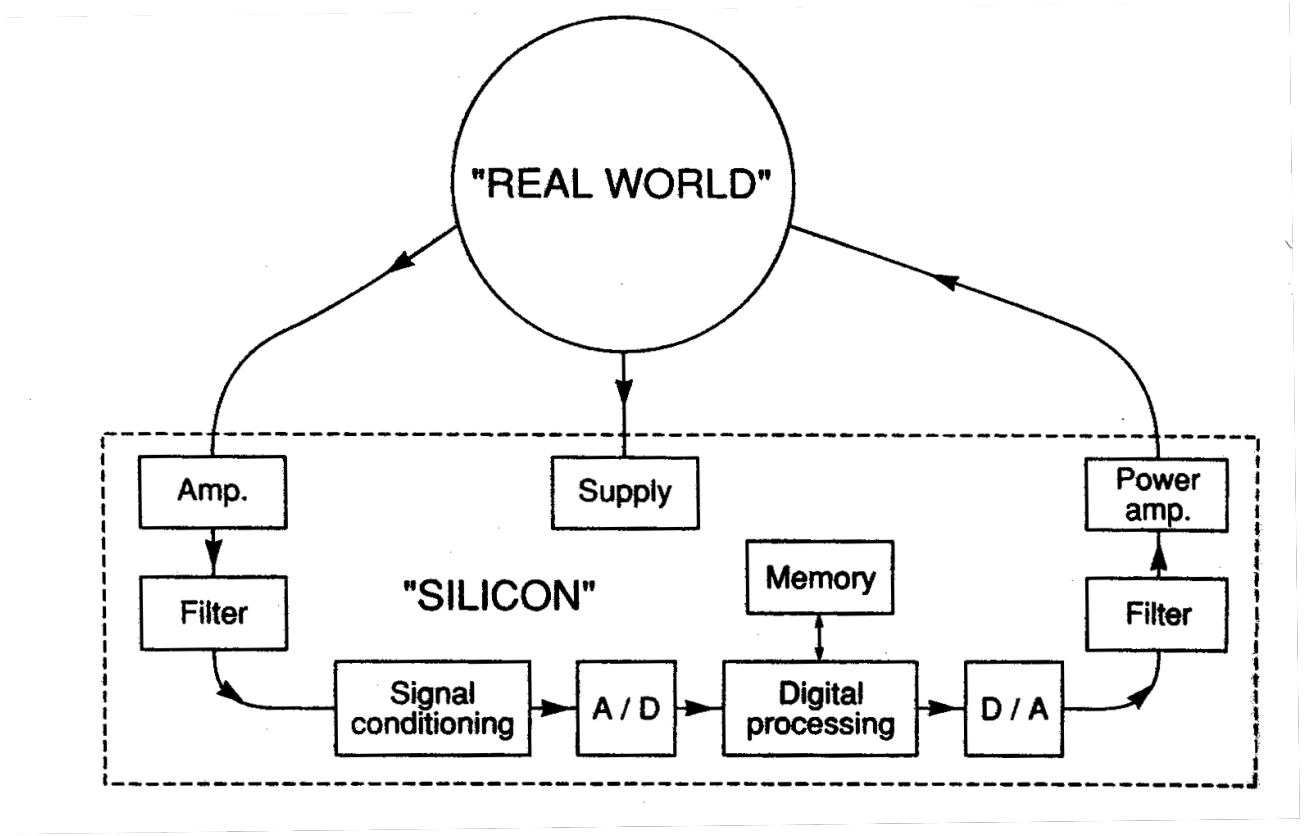
– **Digital filters**



Digital vs. Analog Implementations

☺Programmability.
☺Flexibility.
☺Short design cycles.
☺Good immunity to noise.
☺Good immunity to manufacturing process tolerances.

☹Their performance is degraded in very high frequency applications.

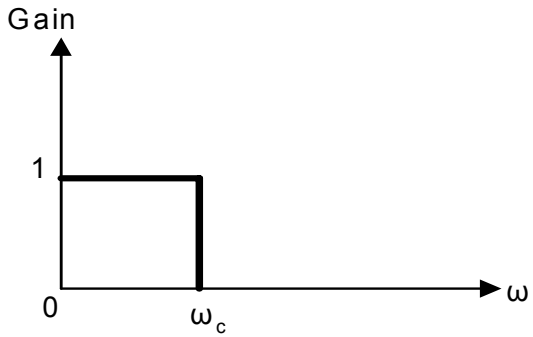


☑ The analog part provides the I/O interface (amplification, filtering, etc.) to the core of the chip which is digital.

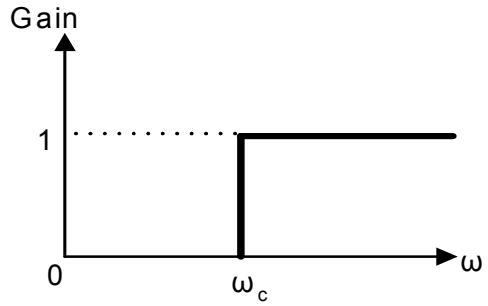
The approximation problem

- Frequency response of ideal filters

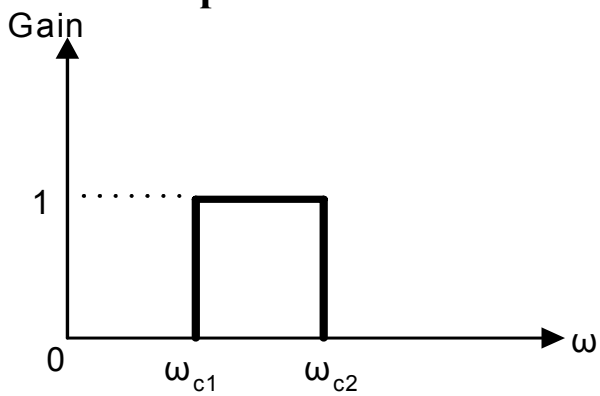
Lowpass filter



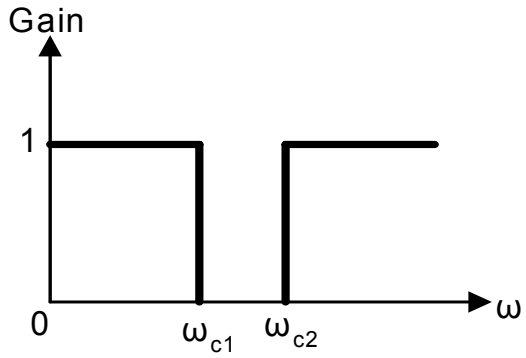
Highpass filter



Bandpass filter

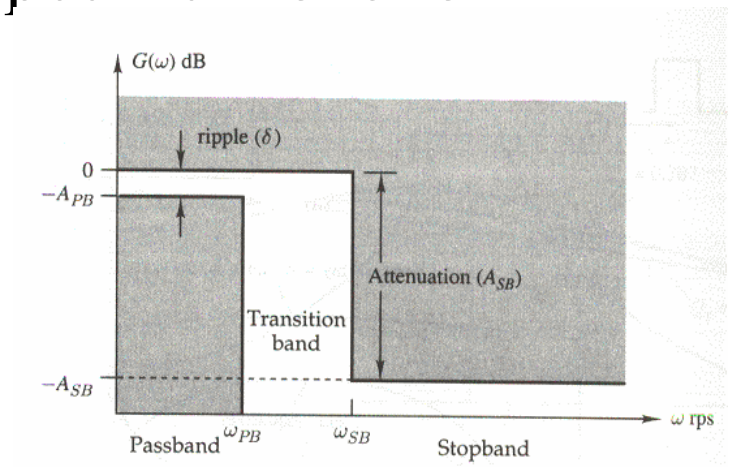


Bandreject filter

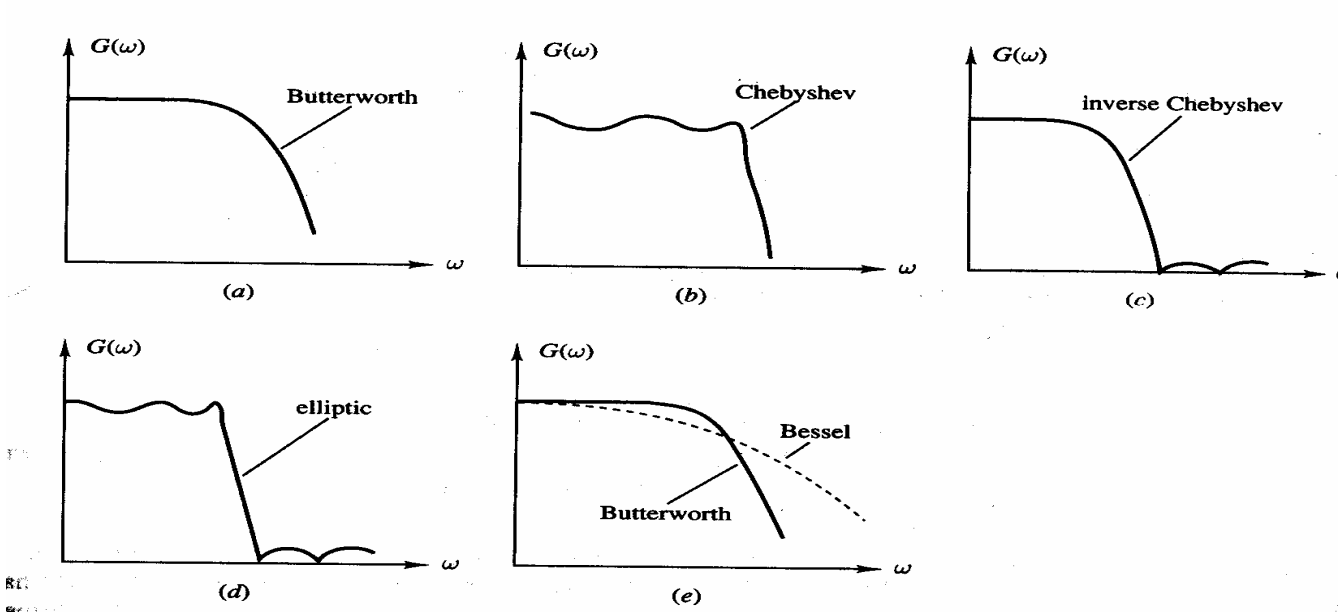


☹ The above responses could not be realized by causal systems.

- Practical specifications for a LP filter



- Characteristic transfer functions.



- **Chebyshev vs Butterworth responses.**

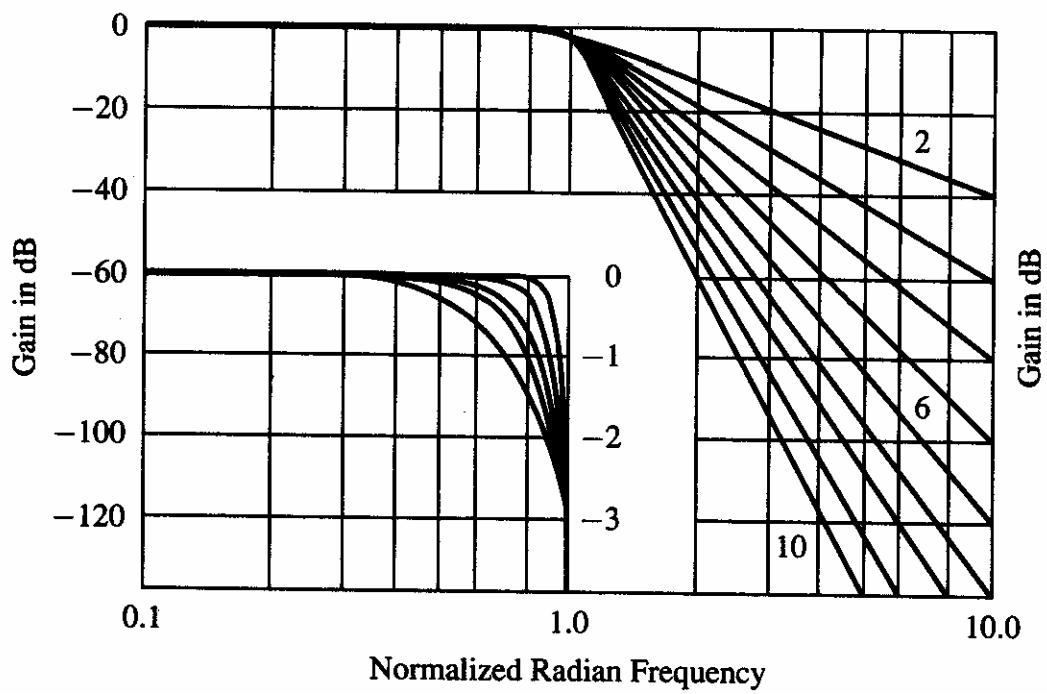
☺ Higher attenuation in stopband.
☺ Steeper roll-off near the cut-off frequency.

☹ More complex filter realizations.
☹ Less linear phase characteristics.

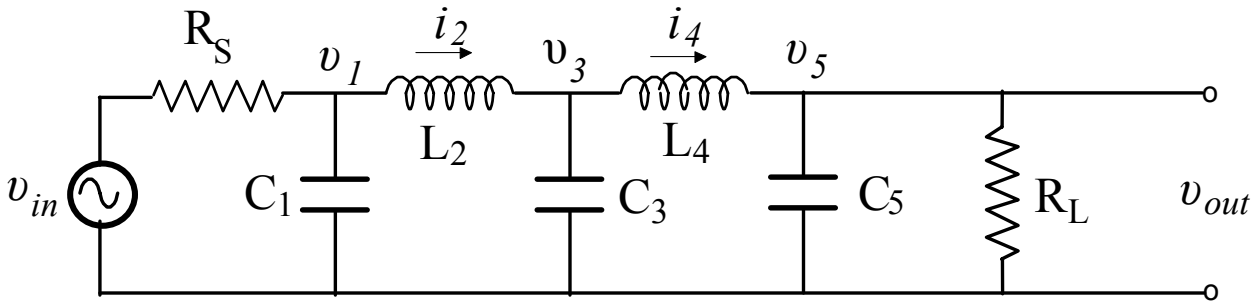
☑ The choice of frequency response that should be implemented, requires trade-off between the above conflicting requirements.

- Determination of the order of a Butterworth filter.

$$N \geq \frac{\log\sqrt{\dfrac{10^{0.1A_{SB}}-1}{10^{0.1A_{PB}}-1}}}{\log\left(\dfrac{\omega_{SB}}{\omega_{PB}}\right)}$$



LC ladder filters



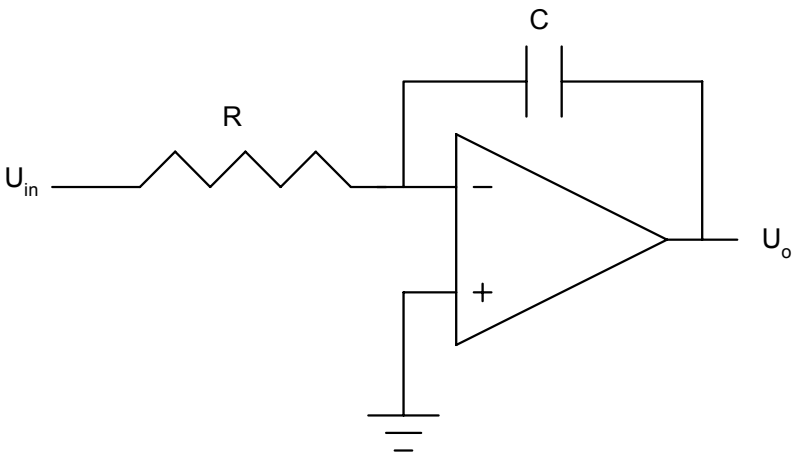
☺A doubly terminated LC ladder has the advantage of low sensitivity to component tolerances.

☺LC ladder filters are mainly used in very high frequency applications.

☹Inductors are heavy and bulky and thus they are difficult to adapt to IC realization.

Active RC filters

- Miller integrator



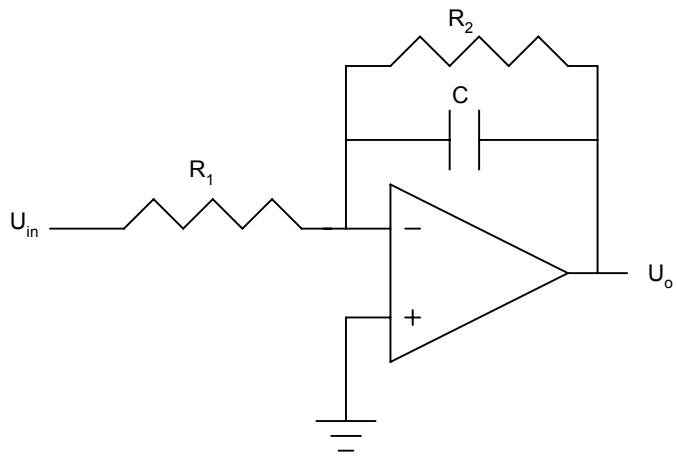
$$H(s) = \frac{U_o(s)}{U_{in}(s)} = -\frac{1}{RCs}$$

Frequency response

$$|H(s)| = \frac{\omega_o}{\omega}, \qquad \omega_o = \frac{1}{RC}$$

ω_o: unity-gain frequency

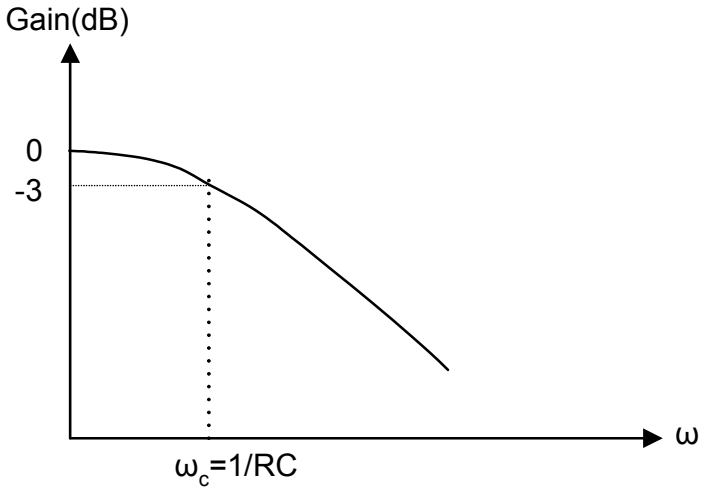
- **First-order filters**



$$H(s) = \frac{U_o(s)}{U_{in}(s)} = -\frac{R_2}{R_1}\frac{1}{R_2 C s + 1}$$

Frequency response

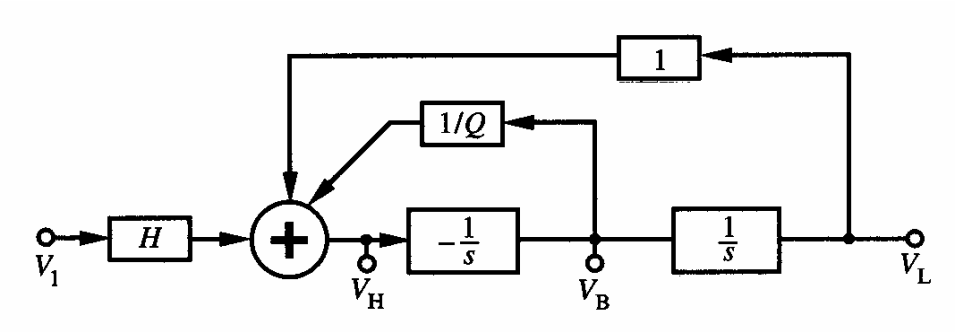
$$|H(j\omega)| = \frac{R_2}{R_1}\frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_c}\right)^2}}$$



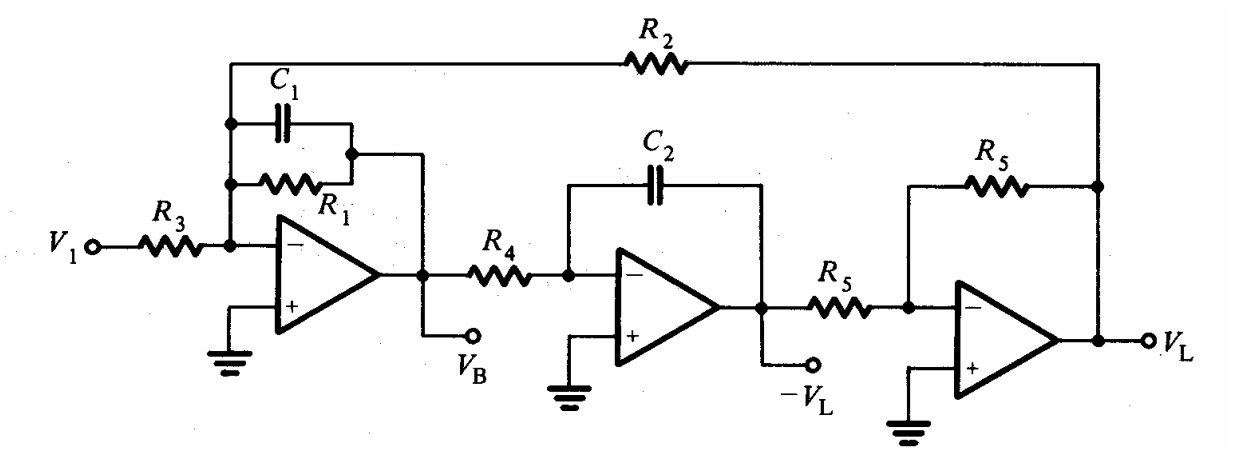
☑ The cutoff frequency is determined by the integrator's time constant.

- Second-order filters (Biquads)

They are constructing using two-integrator loop.



Tow-Thomas Biquad



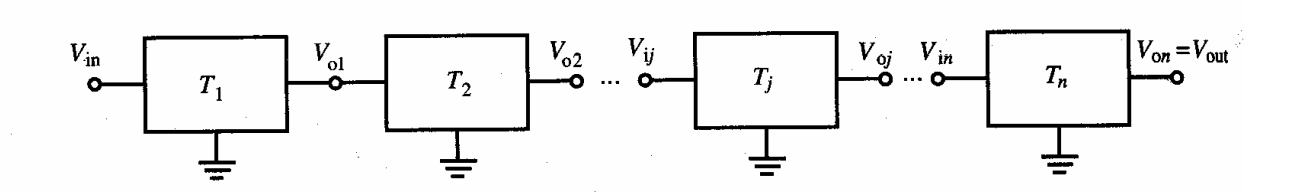
Design of high-order RC filters

- Using second-order sections in cascade connection or with multiple-loop feedback.

- Simulating the corresponding LC ladder prototypes.

  – Functional simulation of LC ladders.
  – Topological simulation of LC ladders.

- **Cascade connection of biquads**



$$T(s) = \prod_{j=1}^{n} T_j(s)$$

Design procedure for maximizing the Dynamic Range

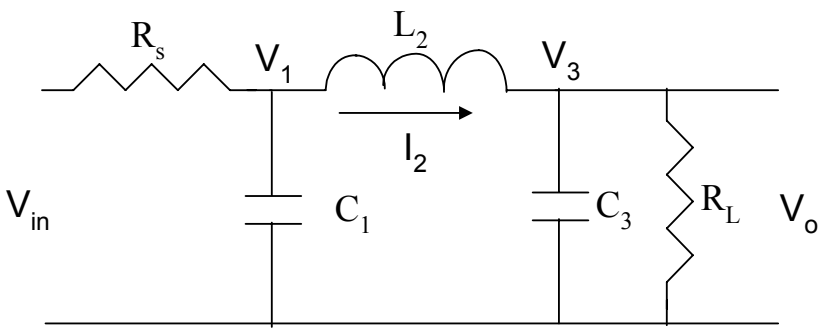
- **Pole-zero pairing:** each pole is assigned to the closest zero.
- **Section ordering:** in the order of increasing values of Q. In addition, LP or BP are employed as first section and HP or BP are employed as last section.
- **Gain assignement:** the gain constants are computed in such a way that the maxima of output voltages of all sections would be made equal.

☺ Easy to design and tune.

☹ Higher sensitivity, in comparison to other filter configurations.

• Functional simulation of LC ladders

✓ **LC ladder prototype**



Voltage/current equations

$$-V_1 = -\frac{1}{sC_1}\left(\frac{V_{in} - V_1}{R_s} - I_2\right)$$

$$-I_2 = -\frac{1}{sL_2}(V_1 - V_3)$$

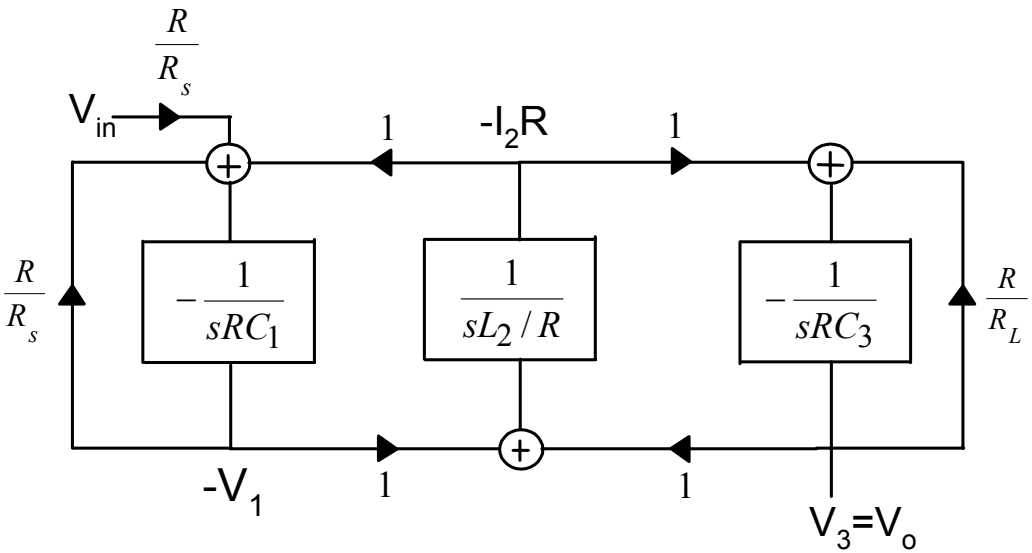
$$V_3 = -\frac{1}{sC_3}\left(\frac{V_3}{R_L} - I_2\right)$$

✓ **Signal Flow Graph (SFG)**

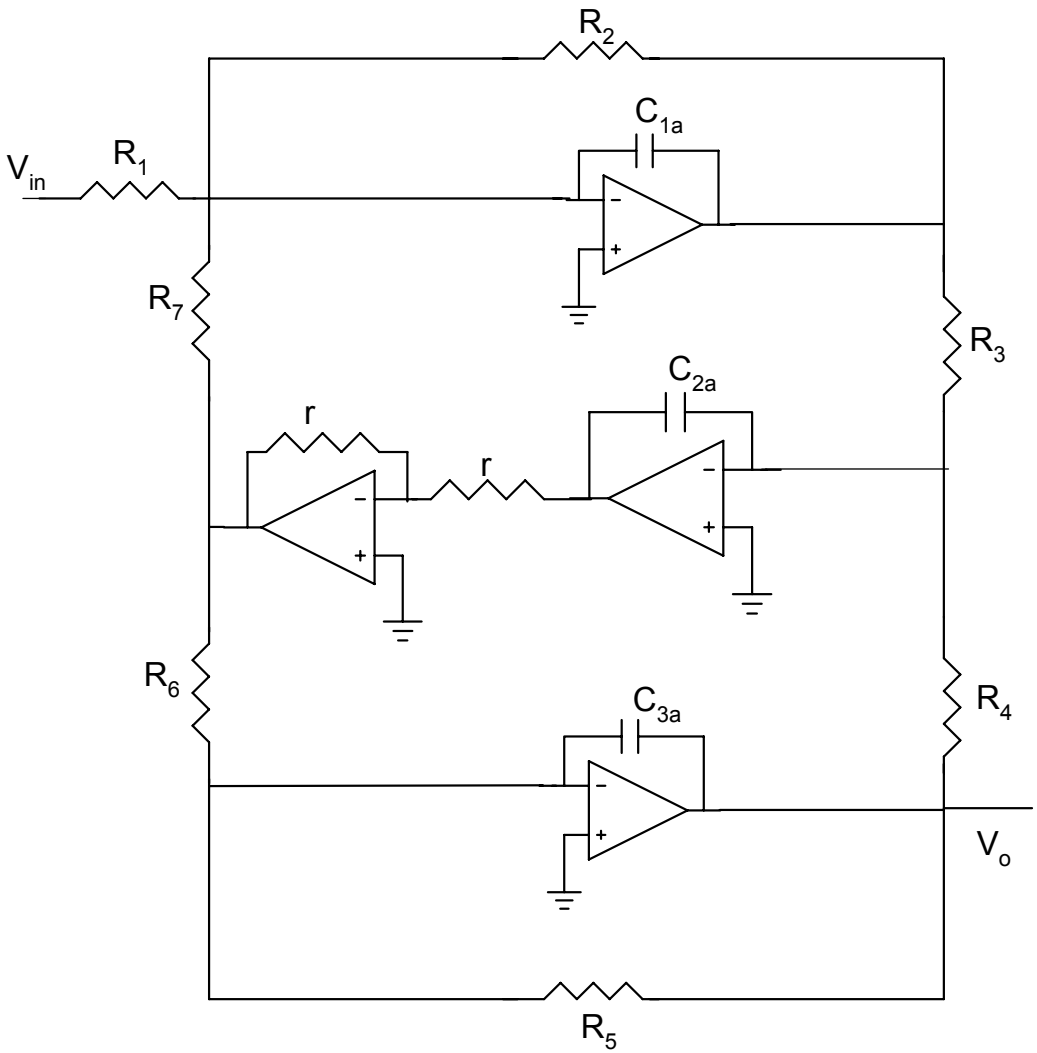
$$-V_1 = -\frac{1}{sRC_1}\left(\frac{R}{R_s}V_{in} - \frac{R}{R_s}V_1 - I_2R\right)$$

$$-I_2R = -\frac{1}{sL_2/R}(V_1 - V_3)$$

$$V_3 = -\frac{1}{sRC_3}\left(\frac{R}{R_L}V_3 - I_2R\right)$$

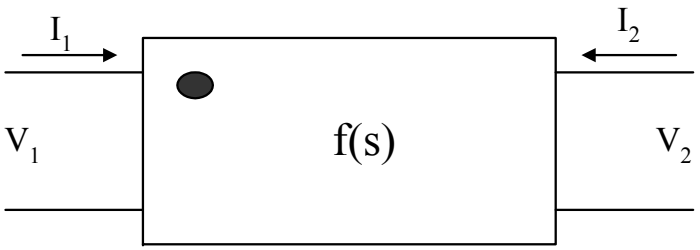


✓ **Active RC filter**



• Topological simulation of LC ladders

• General impedance converter-GIC



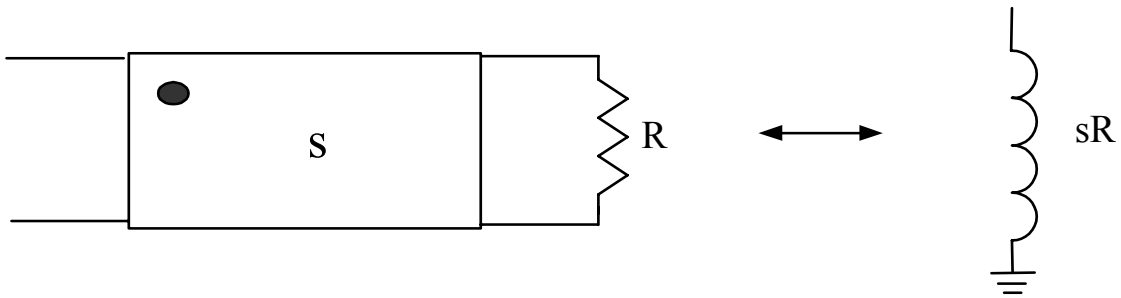
$$V_1 = kV_2$$

$$I_1 = \frac{k}{f(s)} I_2$$

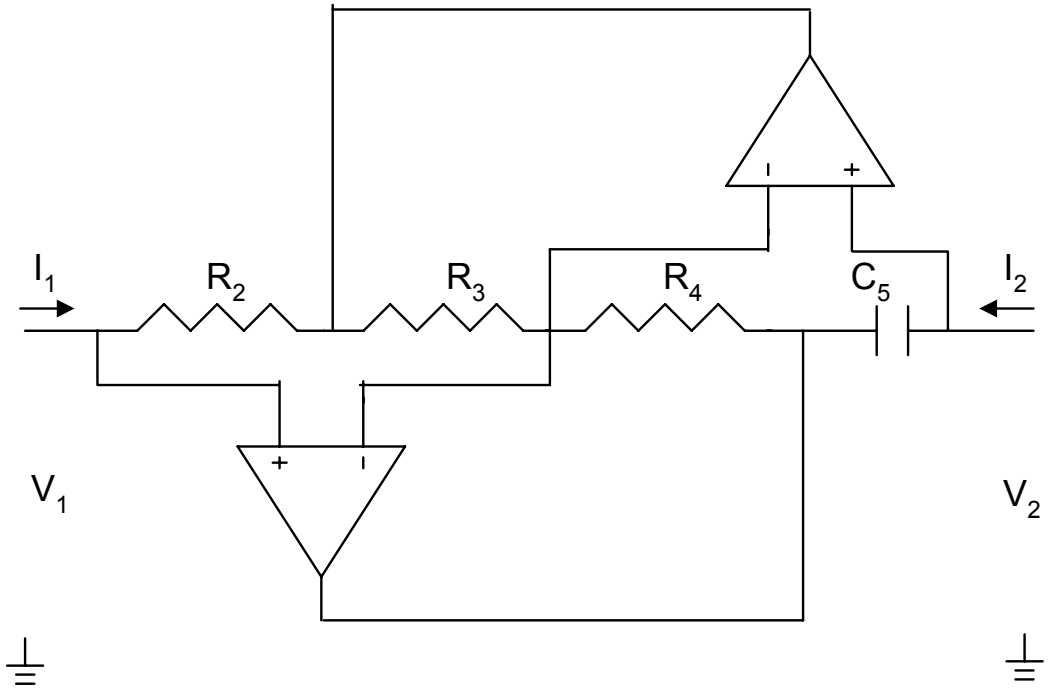
$$Z_{i1} = f(s) \cdot Z_L$$

$$Z_{i2} = \frac{1}{f(s)} Z_s$$

Simulation of a grounded inductance



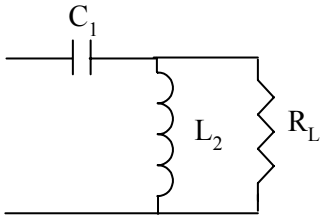
Antoniou circuit



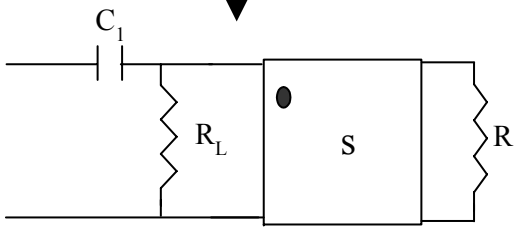
$$f(s) = RCs$$

Steps of design

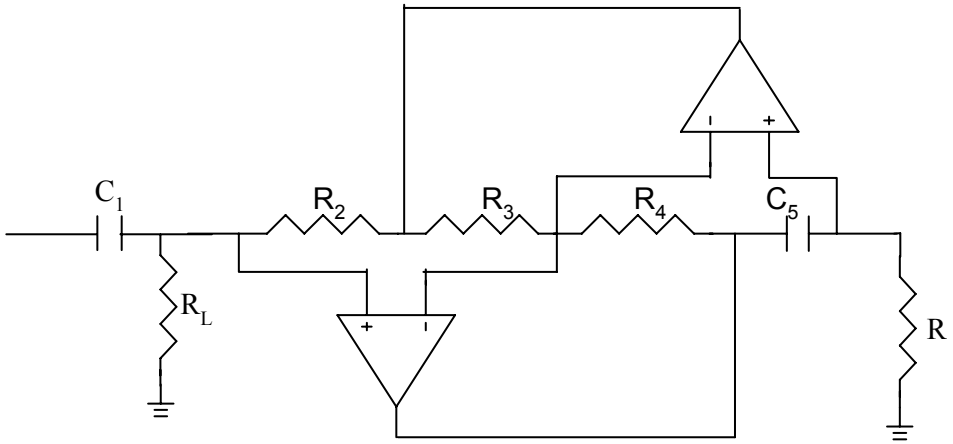
✓ **LC prototype**



✓ **Equivalent circuit using GIC**



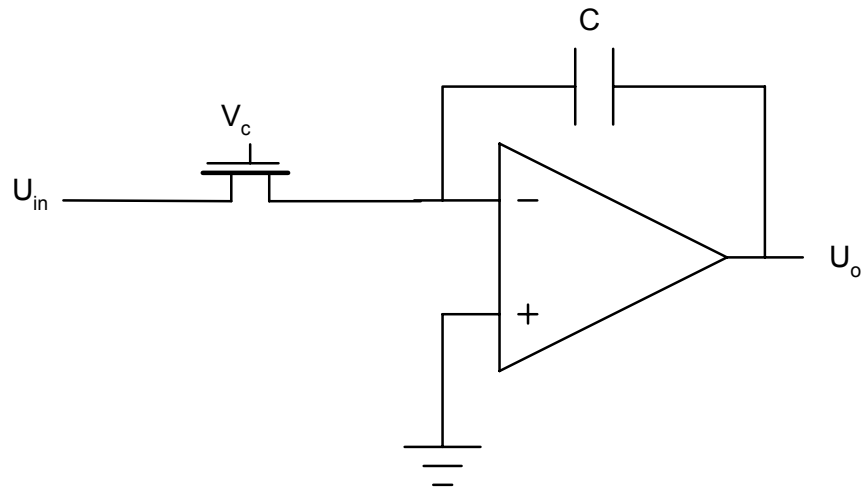
✓ **Active RC filter**



MOSFET-C filters

☹In low-frequency applications (ωc=10*krad/sec*) in case of active RC filters,a resistor with value 5$M\Omega$ is required, in case that C=20pF.

MOSFET-C Miller integrator



☺ Resistors are replaced by MOS transistors operated in linear region. Their values are electronically adjustable by the gate voltage.

☺ The developed active RC design methods can be directly used in MOSFET-C filters.

☹ They suffer from the nonlinearities introduced by MOS transistor.

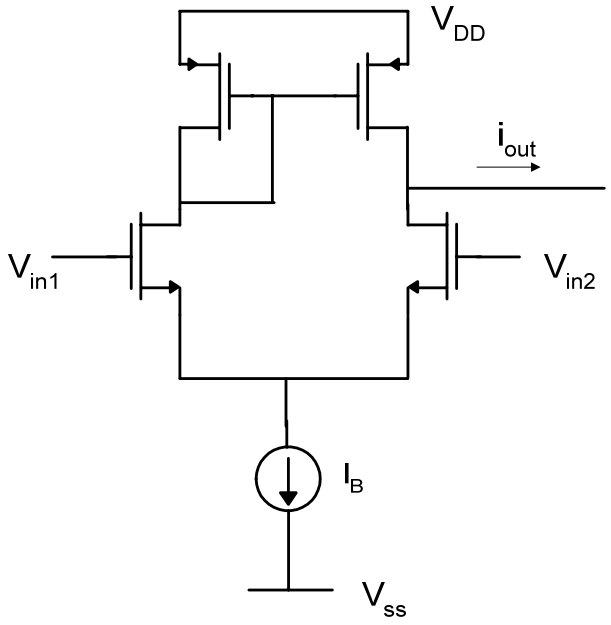
☹ Reduced dynamic range in comparison to active RC filters

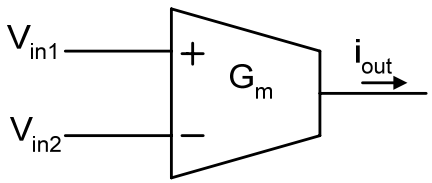
☑ Fully balanced structures are used, in order to reduce the distortion introduced by MOS transistor.

Transconductance-C (G_m-C) filters

☹ The opamp frequency limitations (finite GBW) degrade the performance of active RC, MOSFET-C and SC filters.

Basic CMOS transconductance stage





$$i_{out} = G_m \cdot (V_{in1} - V_{in2})$$

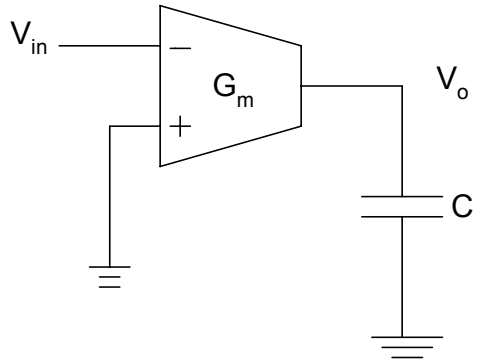
$$G_m = \sqrt{\frac{\mu C_{ox}}{2}\frac{W}{L}}\sqrt{I_B}$$

☺ G_m is electronically adjustable.

☺ The stage has simpler structure, in comparison to the op-amp.

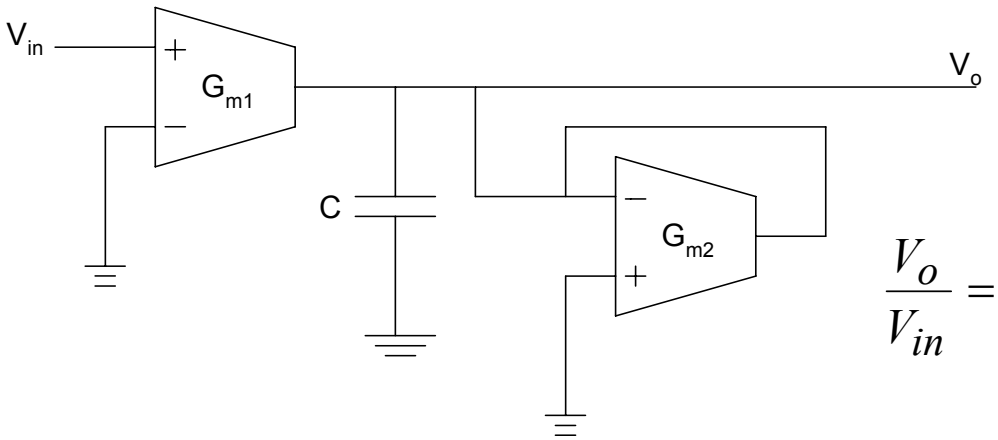
• Basic building blocks for functional simulation of LC ladders & biquads

✓ **Lossless integrator**



$$\frac{V_o}{V_{in}} = -\frac{G_m}{sC}$$

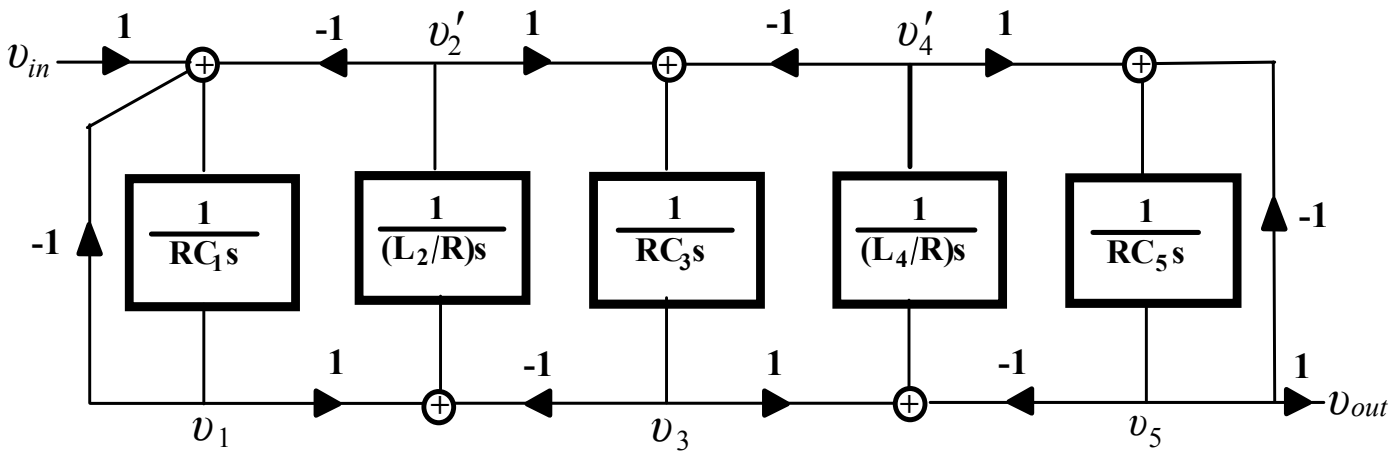
✓ **Lossy integrator**



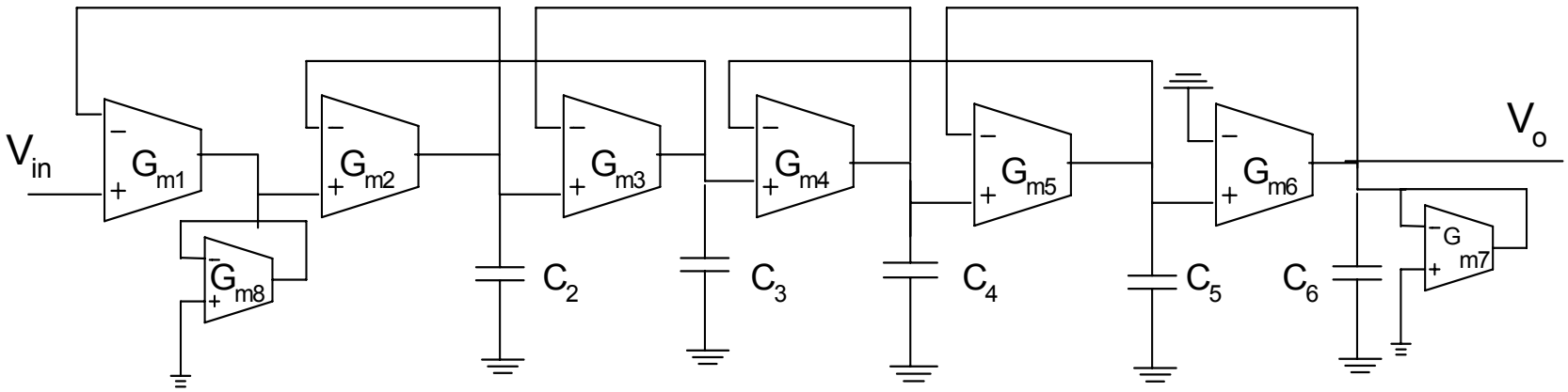
$$\frac{V_o}{V_{in}} = \frac{G_{m1}}{G_{m2}} \frac{1}{\frac{C}{Gm_2} s + 1}$$

▪ 5-th order LP G_m-C filter.

✓ **SFG**

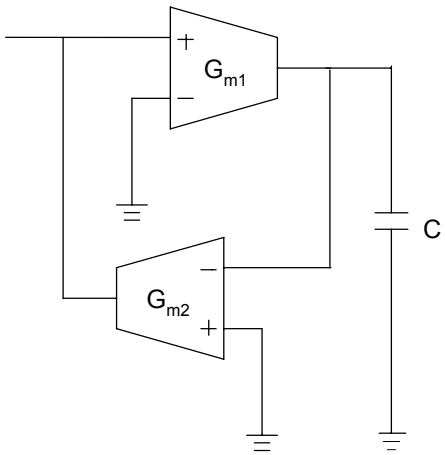


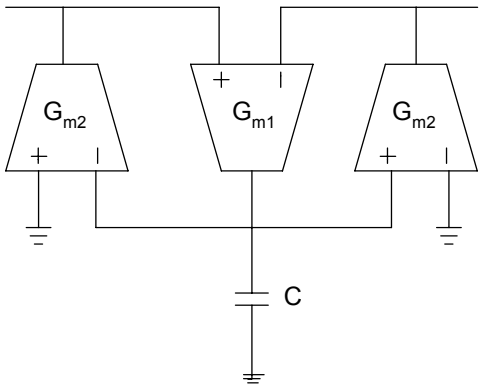
✓ **Configuration of filter**



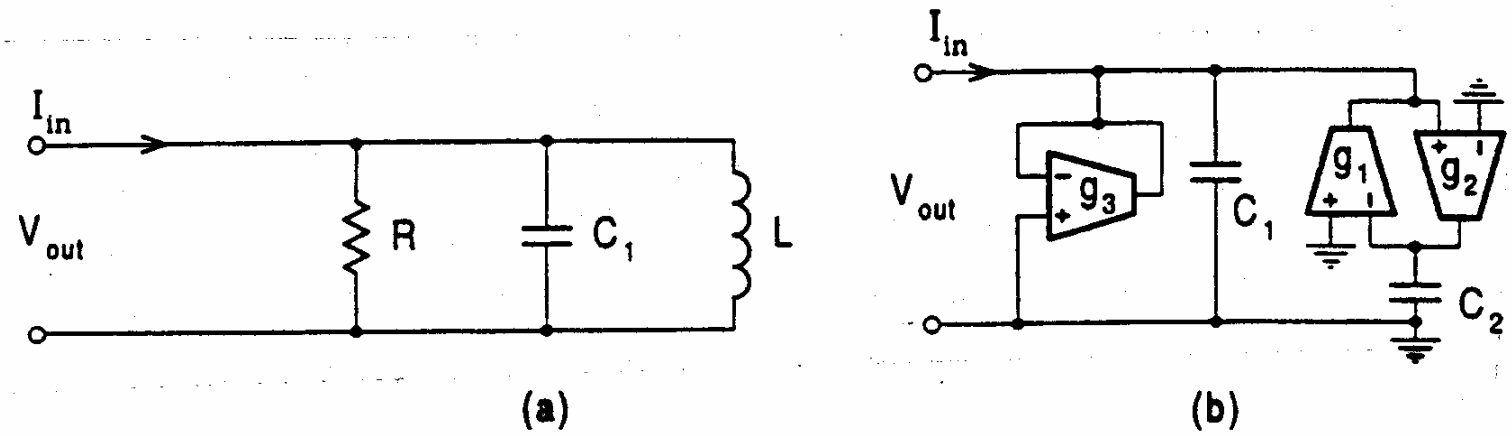
- **Basic building blocks for topological simulation of LC ladders**

✓ **Inductance simulation**



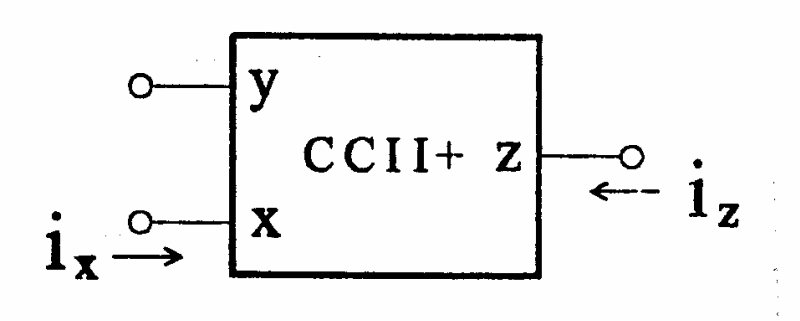


$$L_{eq} = \frac{C}{G_{m1}G_{m2}}$$



Current-Conveyor (CCII) filters

Definitions for CCII



$$\upsilon_x = \upsilon_y$$

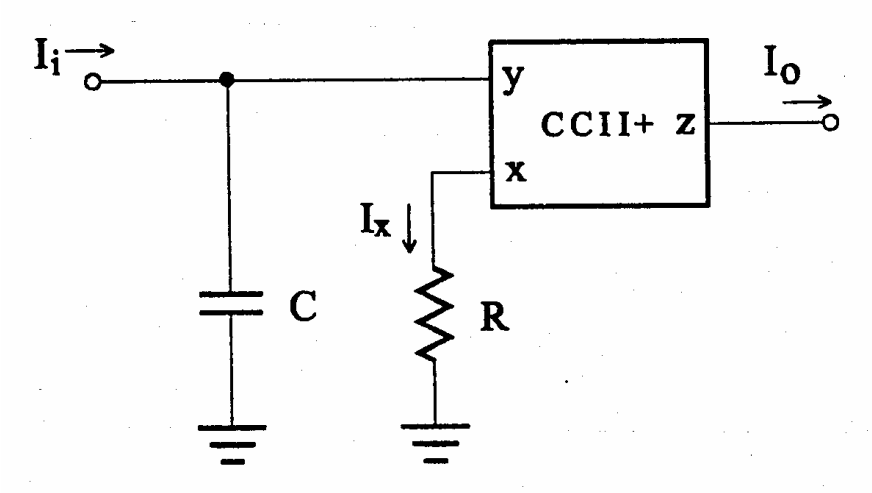
$$i_z = i_x$$

$$R_y \to \infty$$

$$R_x \to 0$$

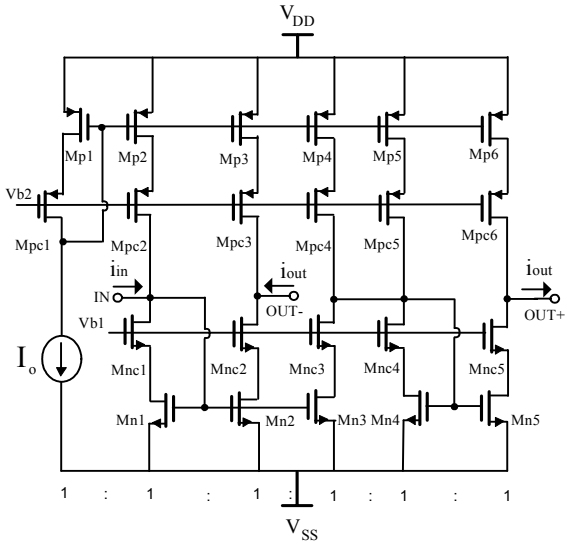
$$R_z \to \infty$$

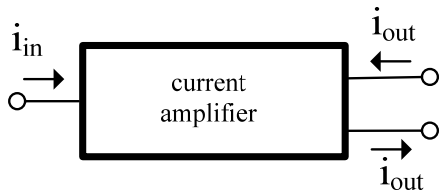
- **CCII lossless integrator**



$$H(s) = \frac{I_o(s)}{I_i(s)} = \frac{1}{RCs}$$

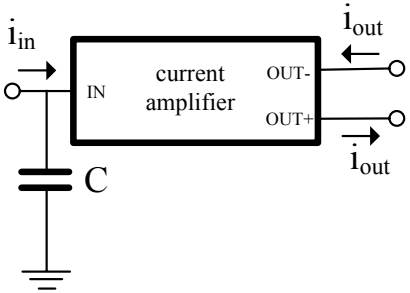
Current Amplifier filters





$$i_{out} = A \cdot i_{in}$$

- **Lossy integrator**



$$H(s) = \frac{1}{1 + RCs}$$

$$R = 1 / g_m$$

$$g_m = \sqrt{2K\frac{W}{L}}\sqrt{I_o}$$

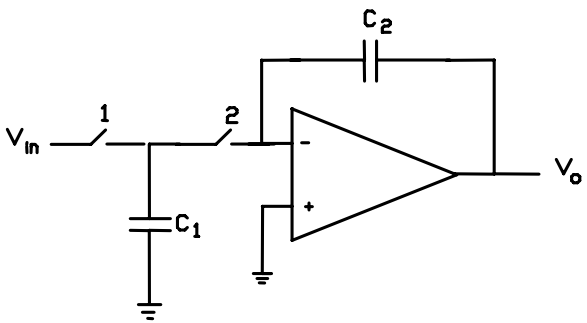
☺ The time-constant of integrator can be electronically adjusted

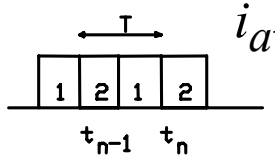
Switched-Capacitor (SC) filters

☹ The time-constants in active RC circuits could not be accurately implemented on chip.

☹ Large resistor values are needed in case of low-frequency applications.

SC integrator





$$i_{av} = \frac{C_1 V_{in}}{T} = \frac{V_{in}}{T / C_1}$$

$$R_{eq} = \frac{T}{C_1}$$

☺ The time-constant is: $\tau = T \cdot \frac{C_2}{C_1}$

☺ The time-constant of integrator is defined by capacitors ration and thus the achieved accuracy is 0.1%.

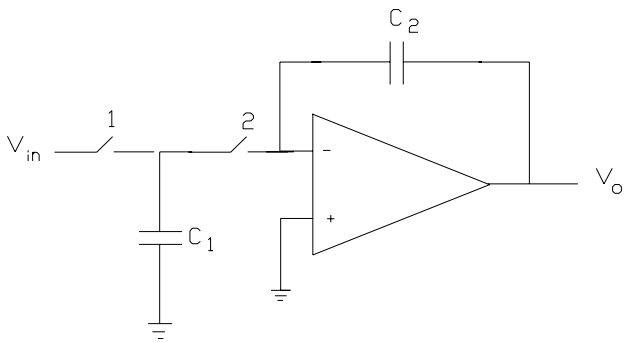
☺ Tuning is achieved using that clock frequency.

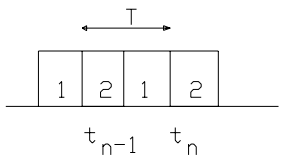
☺ For a resistor value of $10M\Omega$, and using 100kHz clock, a capacitor $1pF$ is needed.

☹ The previous direct replacement of resistors by switched capacitors is valid only in case that the clock frequency is much higher than the signal frequency.

☹ The frequency limitations of op-amps degrade the performance of SC filters.

☺SC filters were designed using s-z transformations.





$$\Delta q_1(tn) = C_1 \upsilon_{in}(t_n - \frac{T}{2})$$

$$\Delta q_2(t_n) = -C_2[\upsilon_o(t_n) - \upsilon_o(t_n - T)]$$

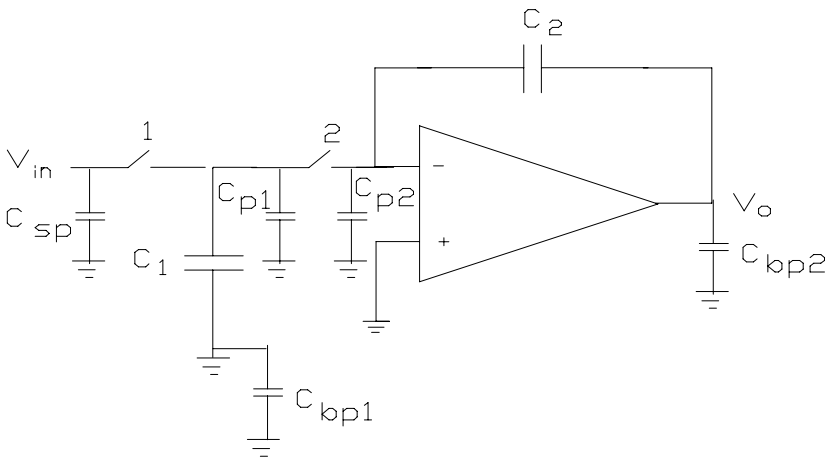
$$\Delta q_1(t_n) = \Delta q_2(t_n)$$

$$H_{1/2}(z) = \frac{V_o(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{z^{-1/2}}{1 - z^{-1}}$$

Setting $z = e^{j\omega}$:

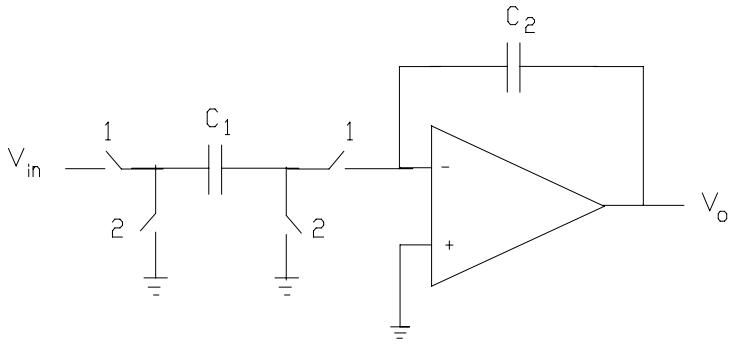
$$H_{1/2}(\omega) = -\frac{C_1/C_2}{j\omega}\frac{\omega/2}{\sin(\omega/2)}$$

☹ The circuit is sensitive to the effect of parasitic capacitances.



$$H_{1/2}(z) = \frac{V_o(z)}{V_{in}(z)} = -\frac{C_1 + C_{p1}}{C_2}\frac{z^{-1/2}}{1 - z^{-1}}$$

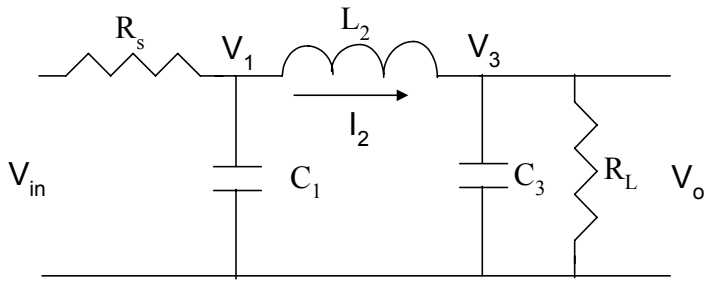
☺ SC integrator insensitive to the effect of parasitic capacitances.



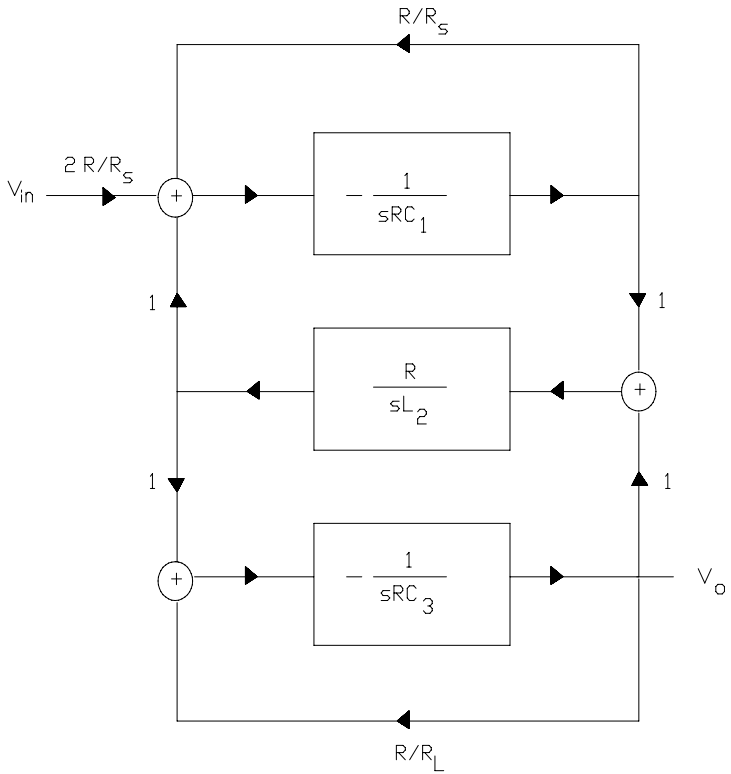
$$H_{1/1}(z) = \frac{V_o(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{1}{1 - z^{-1}}$$

• Steps for designing SC filters

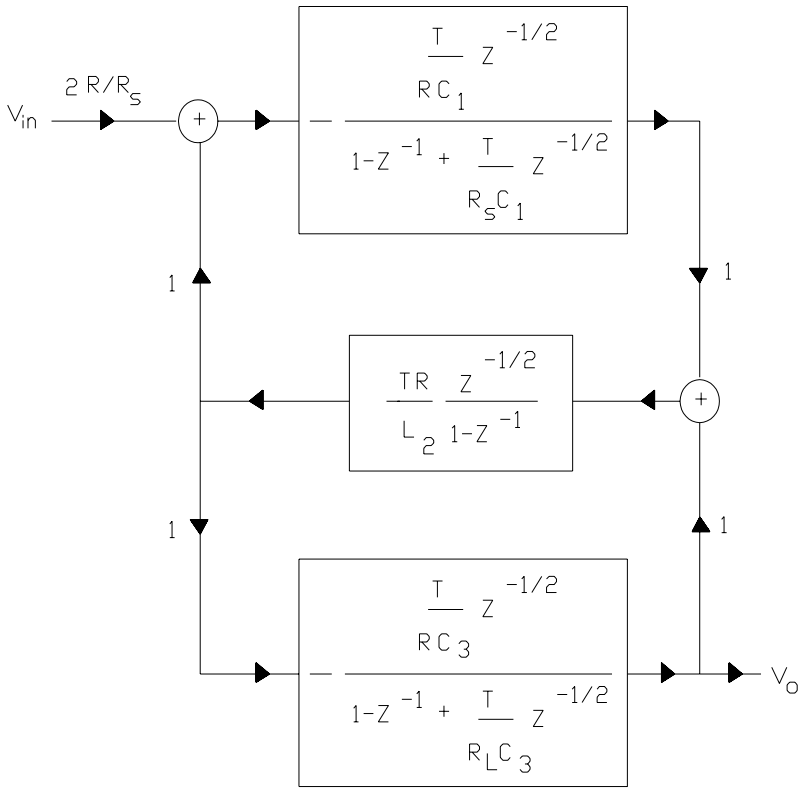
✓ **LC ladder prototype**



✓ **Continuous-time SFG**



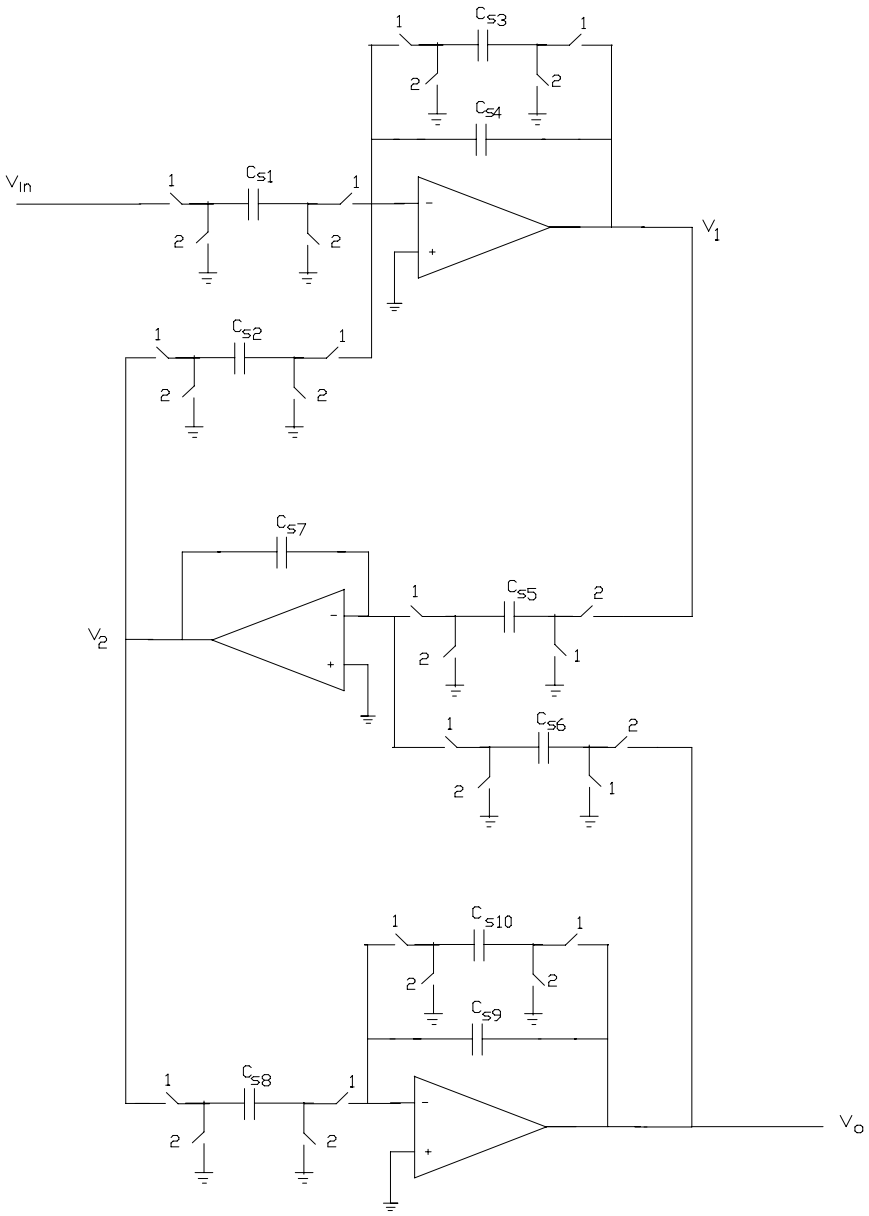
✓ Discrete-time SFG using s-z transformation



The above SFG was derived using the LDI transformation

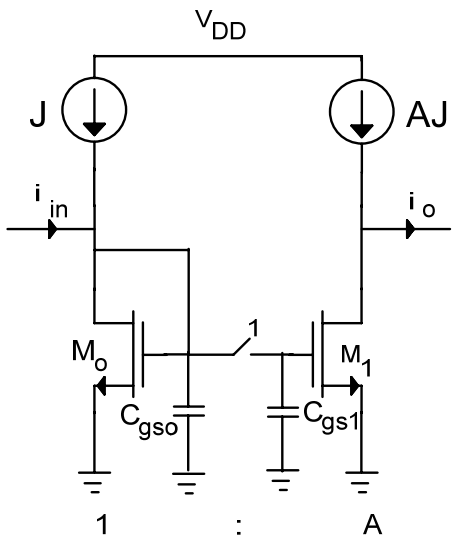
$$s = \frac{1}{T}\frac{1-z^{-1}}{z^{-1/2}}, \qquad \Omega = \frac{2}{T}\sin\left(\frac{\omega}{2}\right)$$

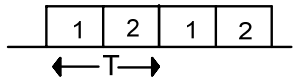
✓ **SC filter**



Switched-Current (SI) filters

Basic memory element





•In time-slot **1** the voltage at gate capacitance is equal to:

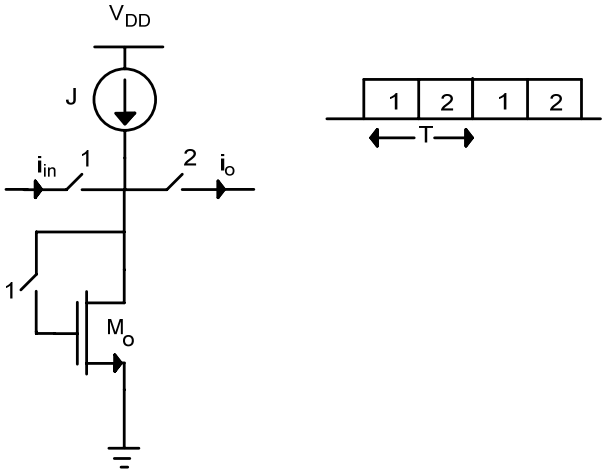
$$\upsilon_{GS} = V_T + \sqrt{\frac{J + i_{in}}{\frac{\mu_o C_{ox} W}{2L}}}$$

•In time-slot **2** transistor M_1 sustains its drain current, and thus:

$$H_{1/2} = \frac{i_o(z)}{i_{in}(z)} = -Az^{-1/2}$$

☺ Capacitors are not further needed and as a result SI filter are fully compatible with standard digital CMOS process.

Dynamic current copier cell

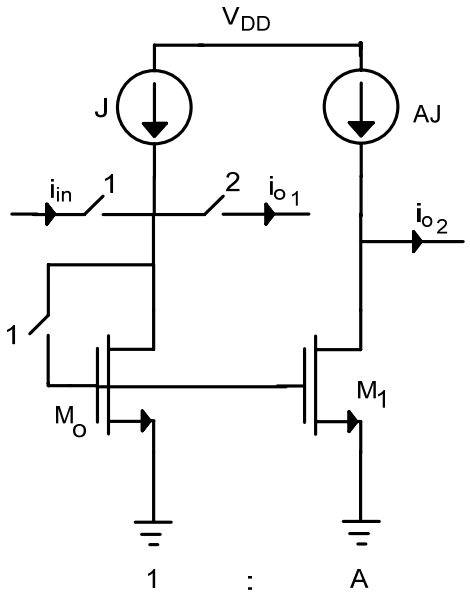


$$H_{1/2} = \frac{i_o(z)}{i_{in}(z)} = -z^{-1/2}$$

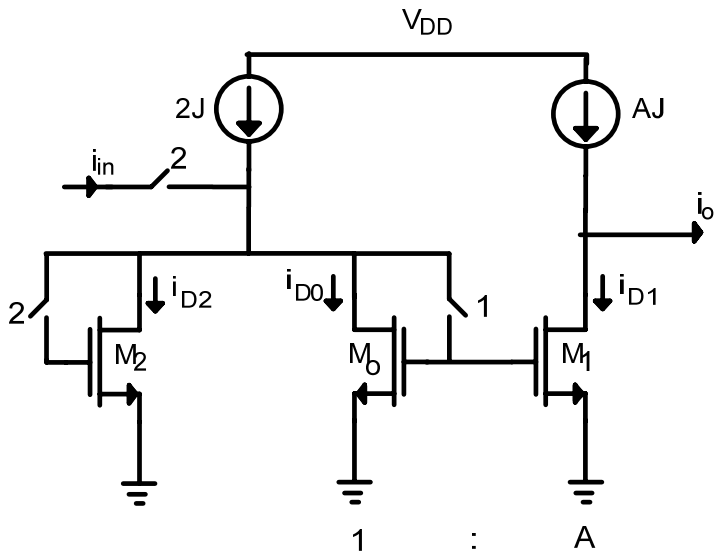
☺ This cell is insensitive to the effect of MOS transistor parameters mismatch.

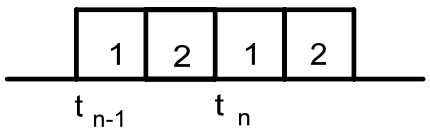
☹ Scaling of output current is not available.

Full period delay cell



- **SI lossless integrator**





Transfer function

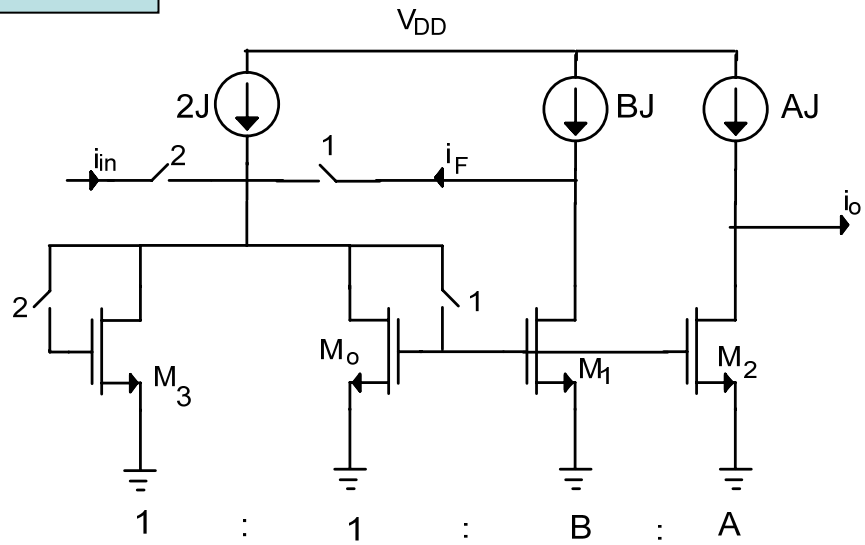
$$H_{1/1}(z) = A\frac{z^{-1}}{1-z^{-1}}$$

Frequency response

$$H_{1/1}(e^{j\omega}) = \frac{A}{j\omega}\frac{\frac{\omega}{2}}{\sin\left(\frac{\omega}{2}\right)}e^{-\frac{j\omega}{2}}$$

☺ The time-constant of integrator is defined by the MOS transistors aspect ratio.

- **SI lossy integrator**



Transfer function

$$H_{1/1}(z) = \frac{\frac{A}{1+B} z^{-1}}{1 - \frac{1}{1+B} z^{-1}}$$

Frequency response

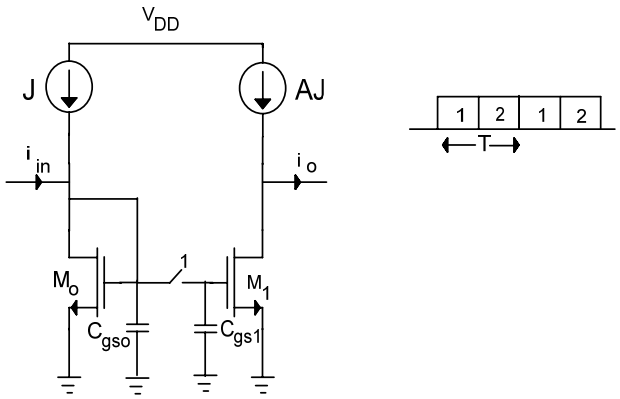
$$H_{1/1}(e^{j\omega}) = \frac{\frac{A}{B}}{1 + j \frac{\omega}{\frac{2}{T}\frac{B}{2+B}}}$$

$$a_o = \frac{A}{B} \quad \text{low frequency gain}$$

$$\omega_o = \frac{2}{T}\frac{B}{2+B} \quad \text{cut-off frequency}$$

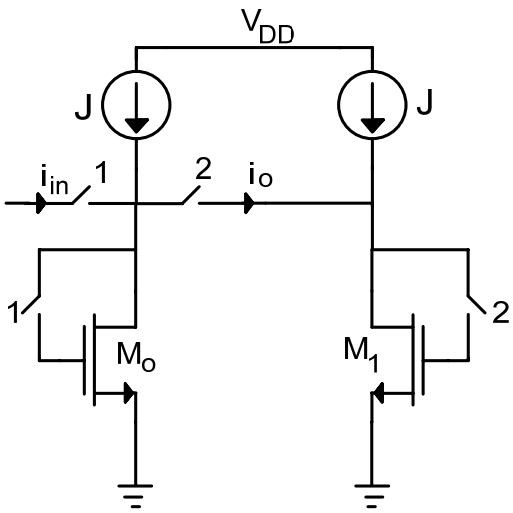
• Effects of non-idealities in SI filters

☹ MOS transistor parameters mismatch



Parameter	DC Offset	Small-Signal Gain Error	Harmonic Distortion
$\Delta K = K_0 - K_1$	$\frac{2(K_0 - K_1)}{K_0 + K_1} J$	$\frac{2(K_0 - K_1)}{K_0 + K_1}$	------
$\Delta W = W_0 - W_1$	$\frac{2(W_0 - W_1)}{W_0 + W_1} J$	$\frac{2(W_0 - W_1)}{W_0 + W_1}$	------
$\Delta L = L_0 - L_1$	$-\frac{2(L_0 - L_1)}{L_0 + L_1} J$	$-\frac{2(L_0 - L_1)}{L_0 + L_1}$	------
$\Delta V_T = V_{T0} - V_{T1}$	$\frac{2(V_{T0} - V_{T1})}{V_{GS0} - V_{T0}} J$	$\frac{(V_{T0} - V_{T1})}{V_{GS0} - V_{T0}}$	$THD \approx \frac{V_{T0} - V_{T1}}{8(V_{GS0} - V_{T0})} \left(\frac{i_{max}}{J} \right)$

☹ Finite input-output conductance ratio of MOS transistor.



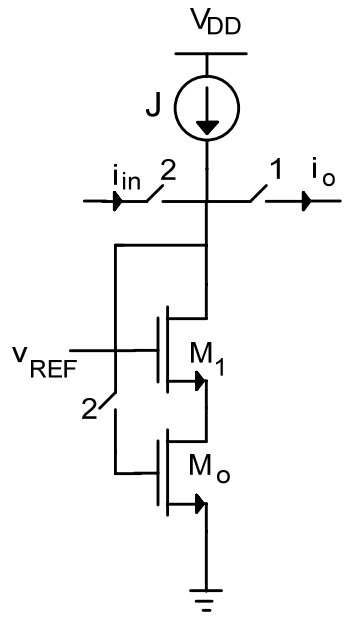
$$H_{2/1}(z) = \frac{i_o(z)}{i_{in}(z)} = -\frac{z^{-1/2}}{1 + \frac{2g_o}{g_i}}$$

$$H_{2/1}(e^{j\omega}) = \frac{H_i(e^{j\omega})}{1 - m(\omega) - j\theta(\omega)}$$

$$m(\omega) = -\frac{2g_o}{g_i}$$

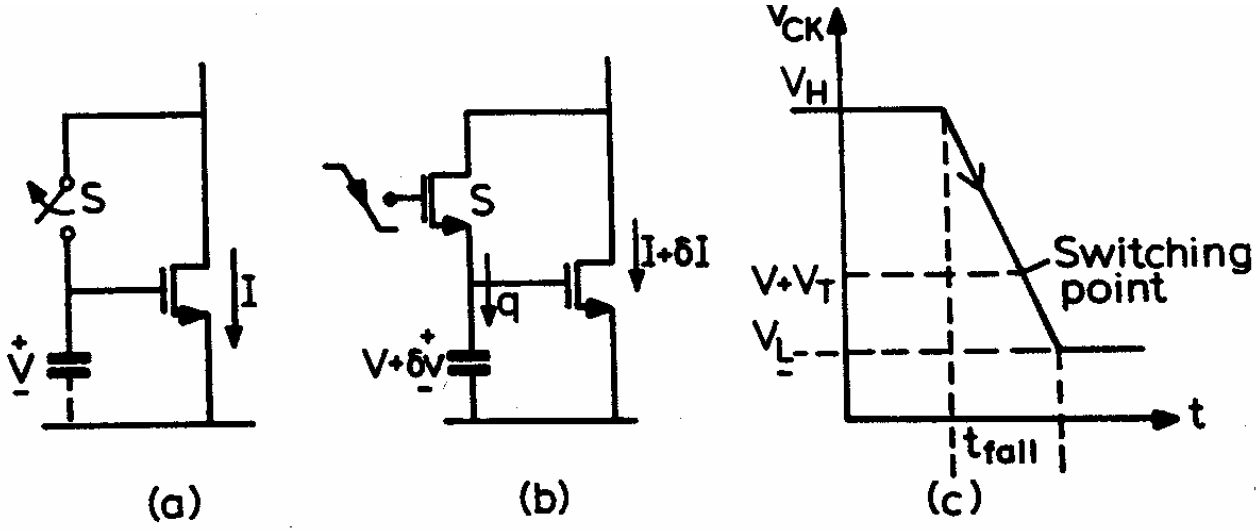
$$\theta(\omega) = 0$$

✓Regulated-cascode structures are used



$$g_{oc} \cong g_o \left(\frac{g_{ds1}}{g_{m1}} \right)$$

☹ Clock-feedthrough effect in MOS switches.



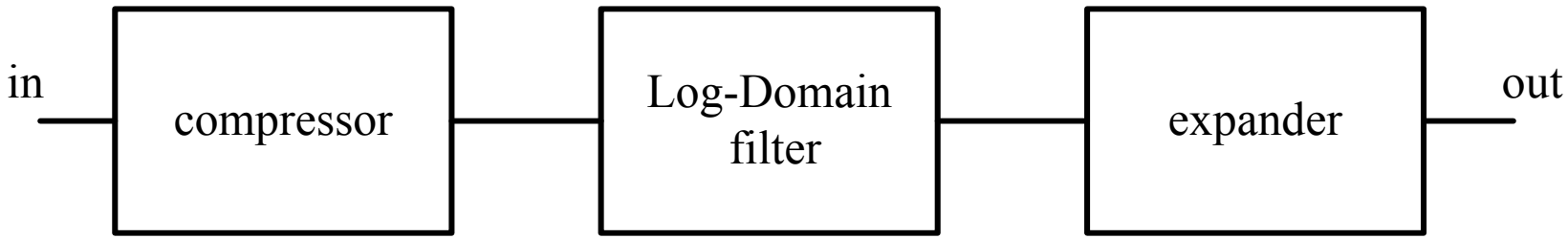
•The error that is caused is similar to that of V_T mismatch.

RFERENCES

1. T. Deliyannis, Y. Sun and J. K. Fidler, “Continuous-time active filter design”, CRC Press, 1999.
2. R. Schaumann and Mc E. Van Valkenburg, “design of active filters”, Oxford University Press, 2001.
3. M. Ismail, T. Fiez “Analog VLSI-Signal and information processing”, McGraw-Hill 1994.
4. C. Toumazou, F. J. Lidgey, and D. G. Haigh,”Analog IC design: the current-mode approach”, IEE Circuits and Systems Series 2, 1990.
5. C. Toumazou, J. B. Hughes and N. C. Battersby,”Switched-currents:an anlog technique for digital technology”, IEE Circuits and Systems Series 5, 1993.
6. M. S. Ghausi and K. R. Laker, “Modern filter design: active RC and switched capacitor”, Englewood Cliffs, NJ:Prentice-Hall Inc., 1981.
7. R. Gregorian, and G.C. Temes, “Analog MOS integrated circuits for signal Processing”, John Willey & Sons, 1986.

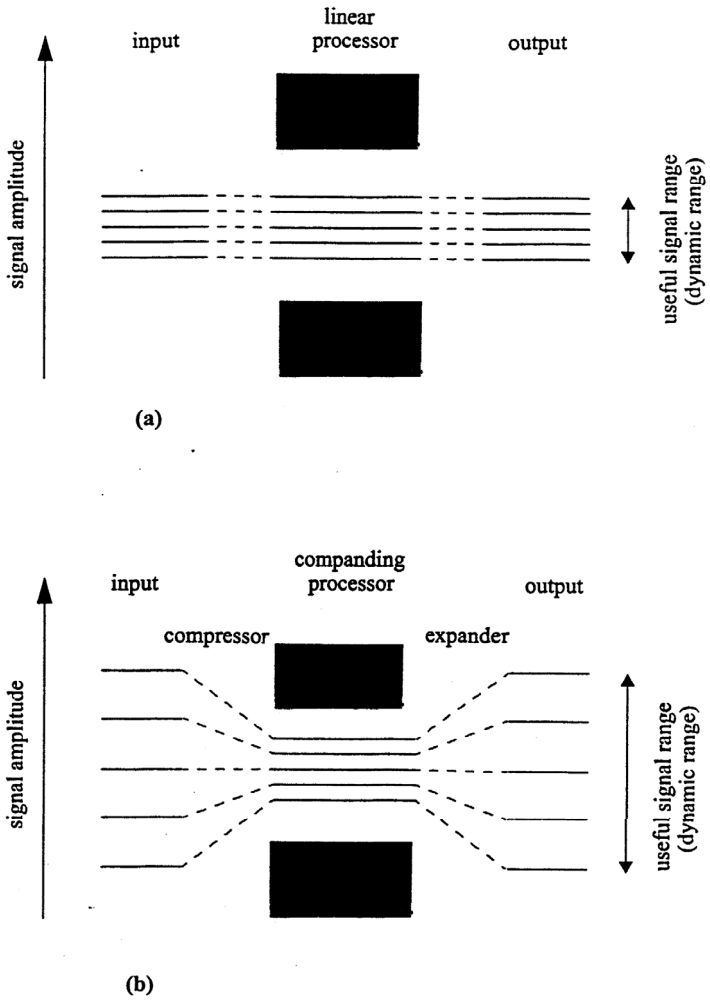
Part-II: Companding filters

INTRODUCTION

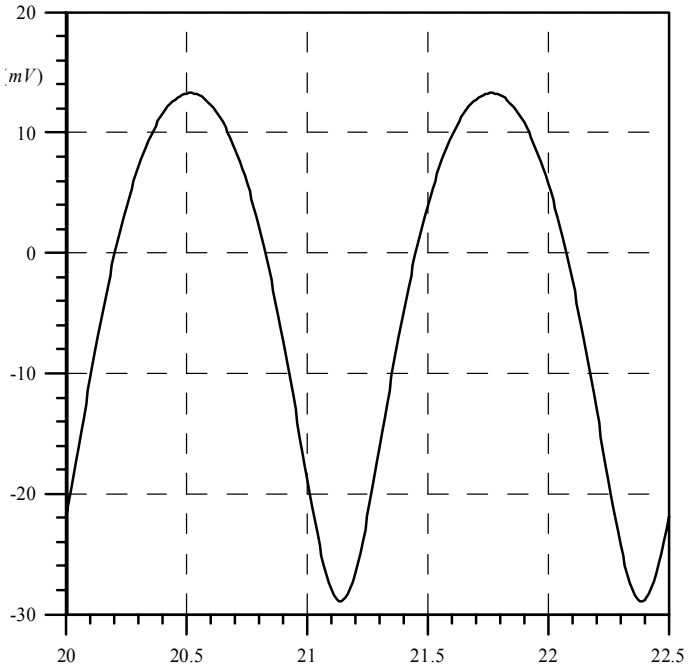


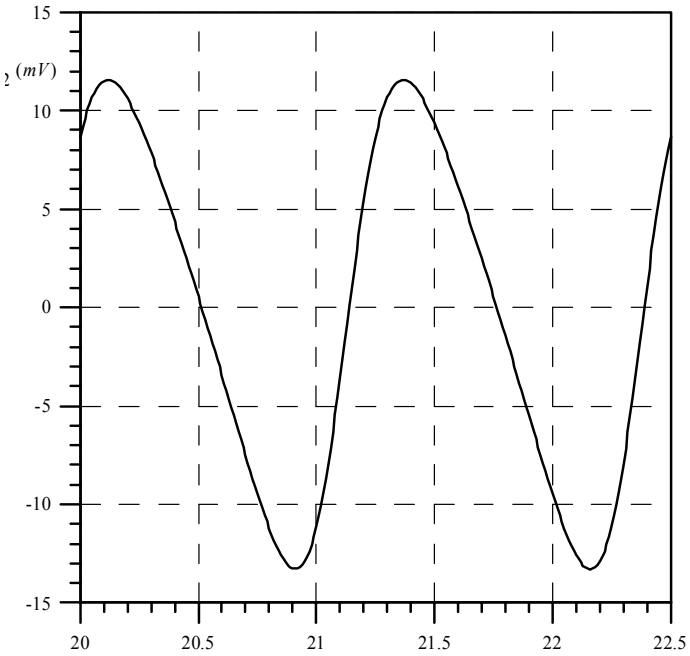
☺ They open the door to elegantly realizing a linear system with inherently non-linear building blocks, and may achieve the advantageous potential of companding (compress-expand) signal processing.

•Linear and companding signal processing



- Waveforms at the internal nodes of a typical log-domain system.





☺ Companding filters have potential for low-voltage operation, as the signal swings within filter are typically less than 100mV.

Log-Domain Filters

Methods for designing Log-Domain filters

✓Using the well-known state-space synthesis approach in linear domain, and an appropriate mapping of the resulted equations.

☹ A large number of equations is needed in case of high order filters.

✓Using the well-known Signal Flow Graph (SFG) synthesis approach in linear domain, and a set of complementary operators.

☺This method is more simpler than the ESS.

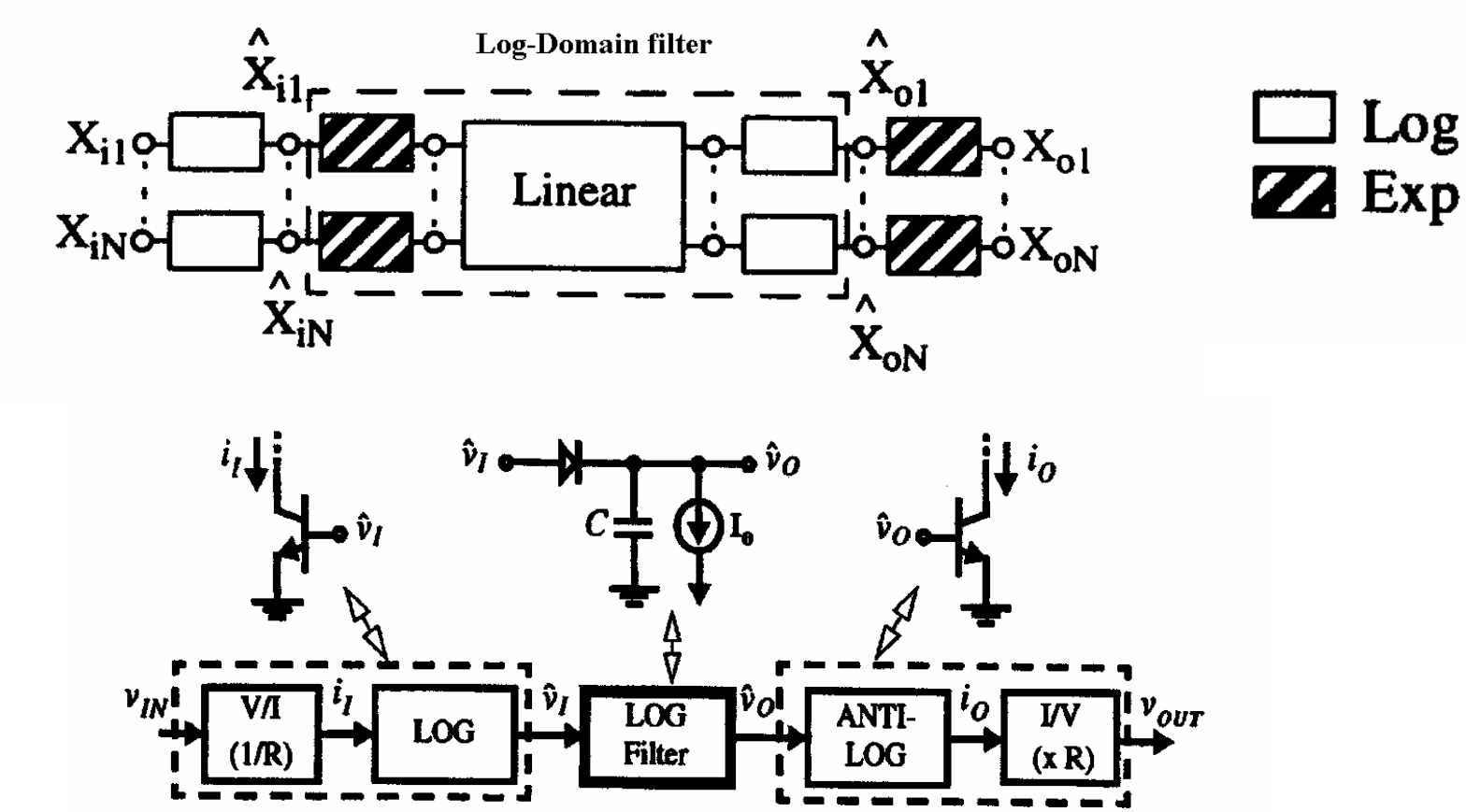
✓By following the concept of Wave Active Filters.

☺ The design procedure of high-order filters is quite facilitated.

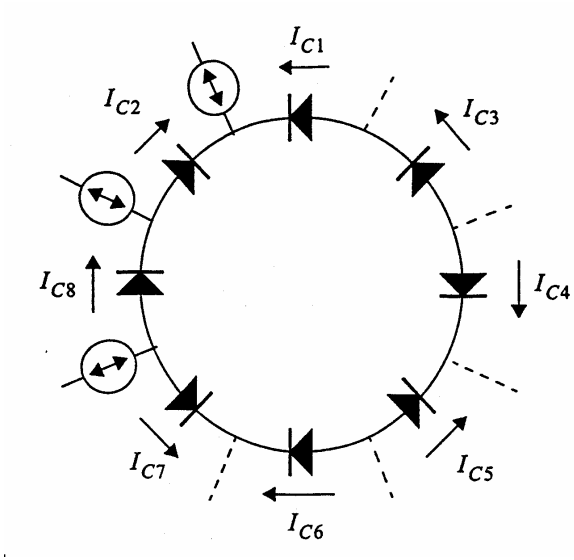
☺ Modular filter structures are derived.

Log-Domain filters synthesis using the SFG approach

Representation of a Log-Domain filter using complementary operators



BJT Translinear principle



✓For any closed loop comprising any number of pairs of clockwise and counter-clockwise forward-biased identical junctions, the product of currents for the elements in one direction is equal to the corresponding product in the opposite direction.

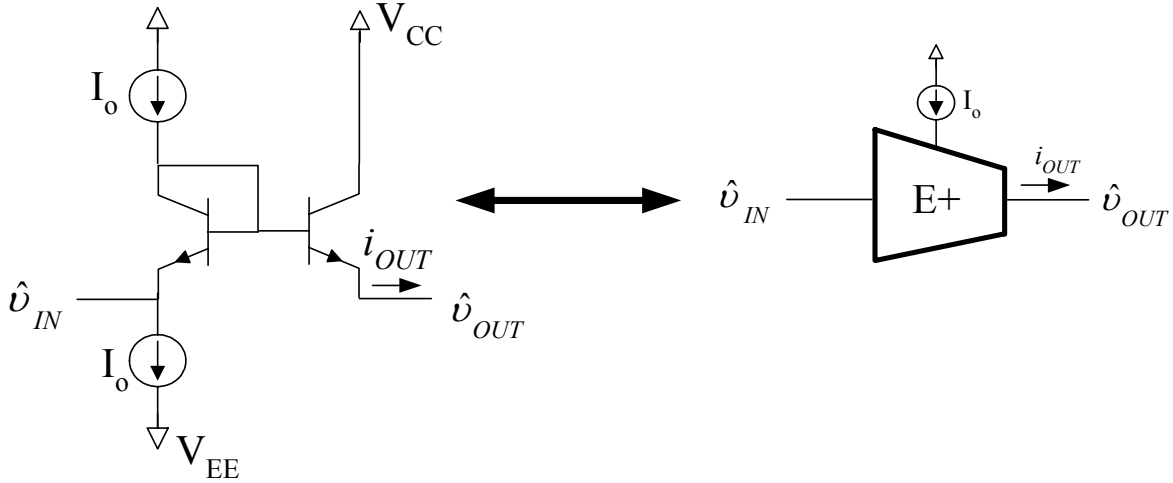
$$\prod_{cw} I_C = \prod_{ccw} I_C$$

- As an extension to the above principle, when a voltage source is introduced into the loop, then:

$$\prod_{cw} I_C = e^{\frac{v_S}{V_T}} \cdot \prod_{ccw} I_C$$

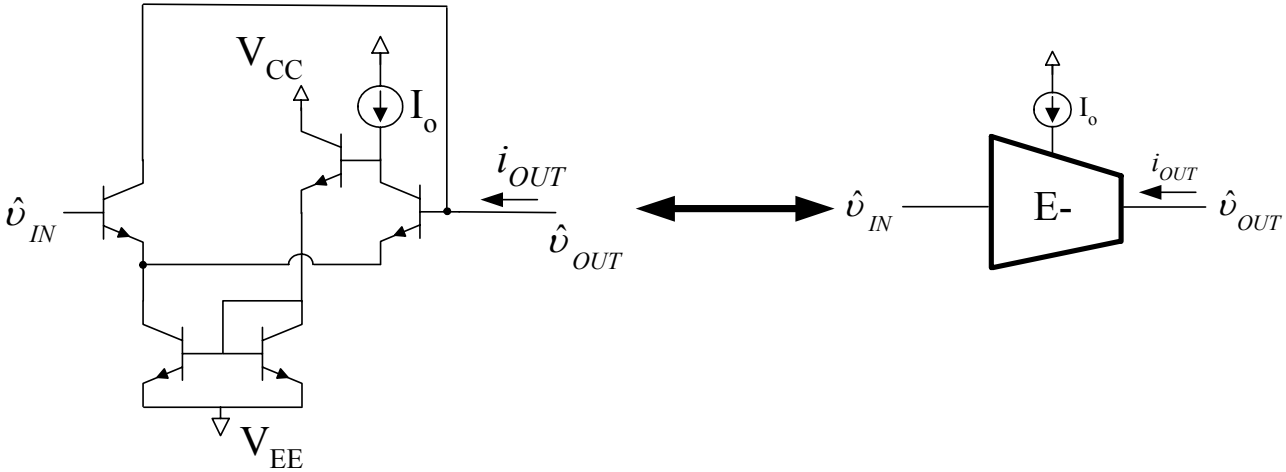
Non-linear transconductance

Positive cell



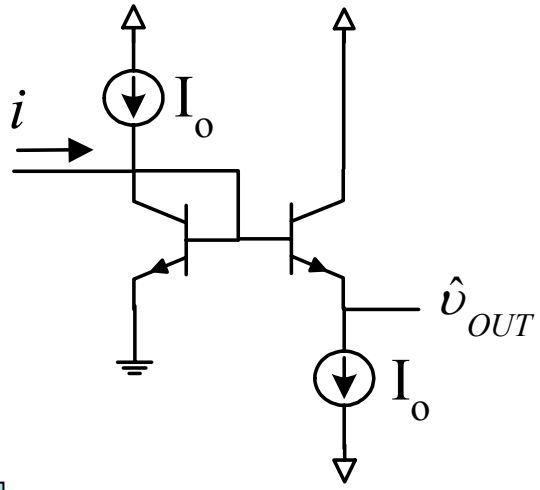
$$i_{OUT} = I_o \cdot e^{\frac{\hat{\upsilon}_{IN} - \hat{\upsilon}_{OUT}}{V_T}}$$

Negative cell

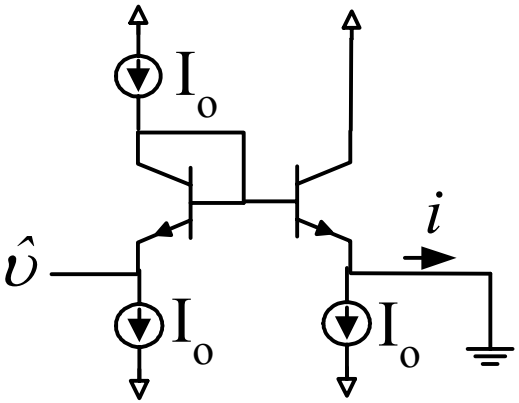


Implementation of complementary operators

LOG



EXP

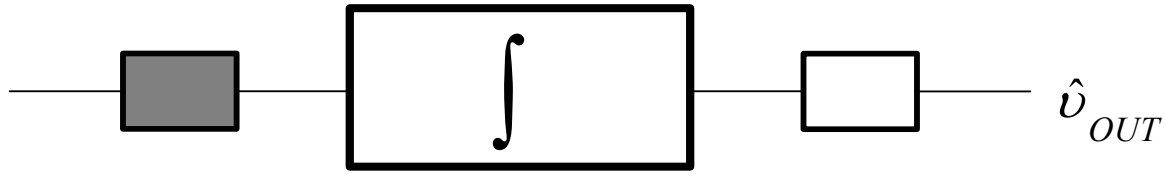


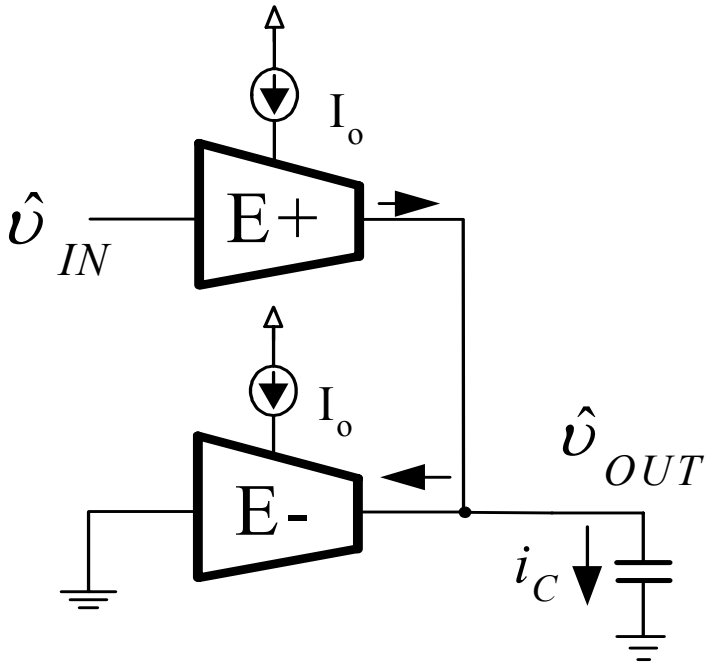
$$EXP(\hat{\upsilon}) = I_o \cdot e^{\frac{\hat{\upsilon}}{V_T}} - I_o$$

$$LOG(i) = V_T \cdot ln\left(\frac{i + I_o}{I_o}\right)$$

Log-Domain integrators

Lossless integrator





$$i_C = C \cdot \frac{d\hat{\upsilon}_{OUT}}{dt} = I_o \cdot e^{\frac{\hat{\upsilon}_{IN} - \hat{\upsilon}_{OUT}}{V_T}} - I_o \cdot e^{-\frac{\hat{\upsilon}_{OUT}}{V_T}}$$

$$EXP(\hat{\upsilon}_{OUT}) = \frac{1}{\tau} \int \left[EXP(\hat{\upsilon}_{IN}) \right] \cdot dt$$

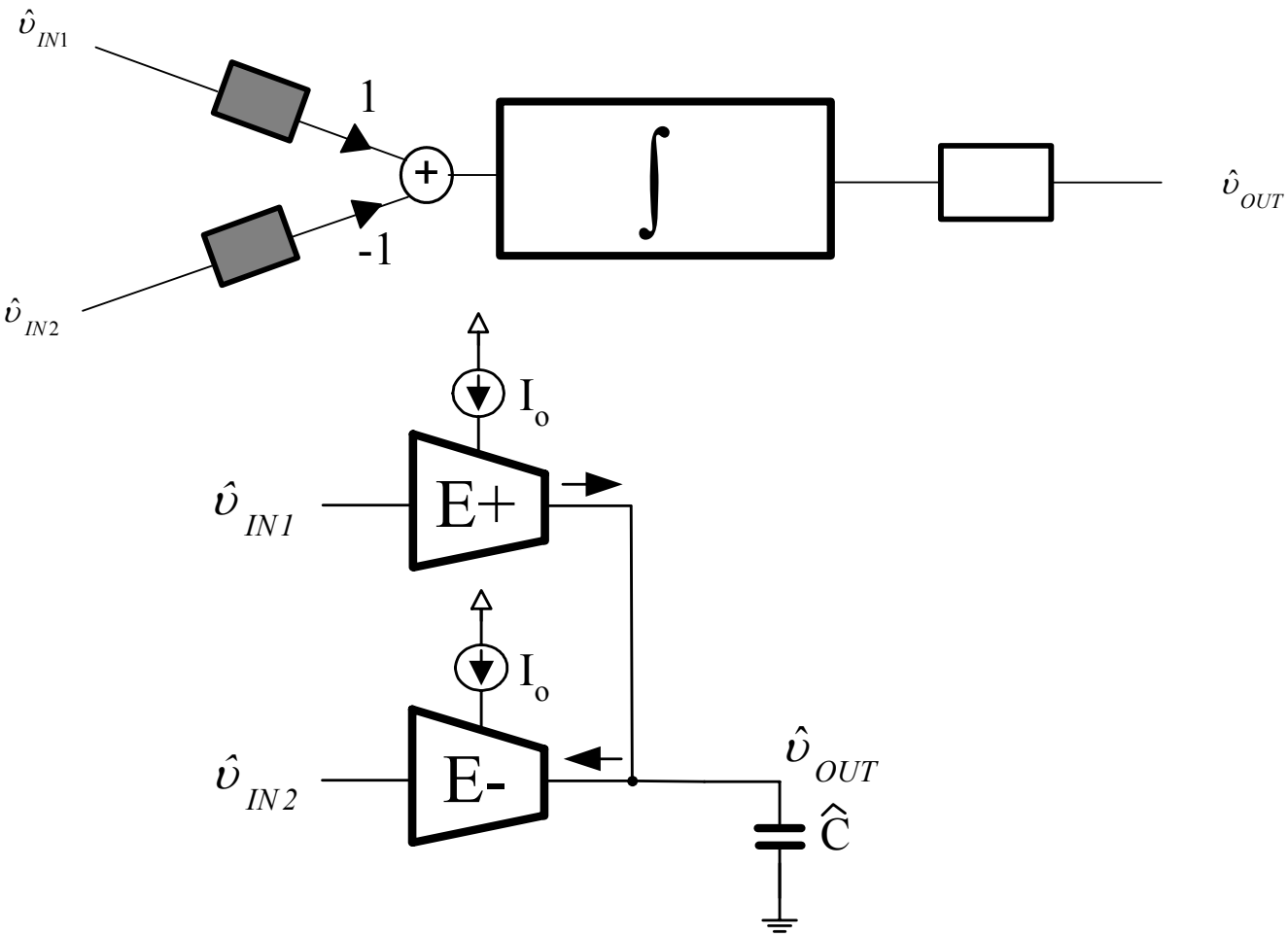
The time-constant of integrator is:

$$\tau = \frac{CV_T}{I_o}$$

☺ Electronic tuneability using a DC current source.

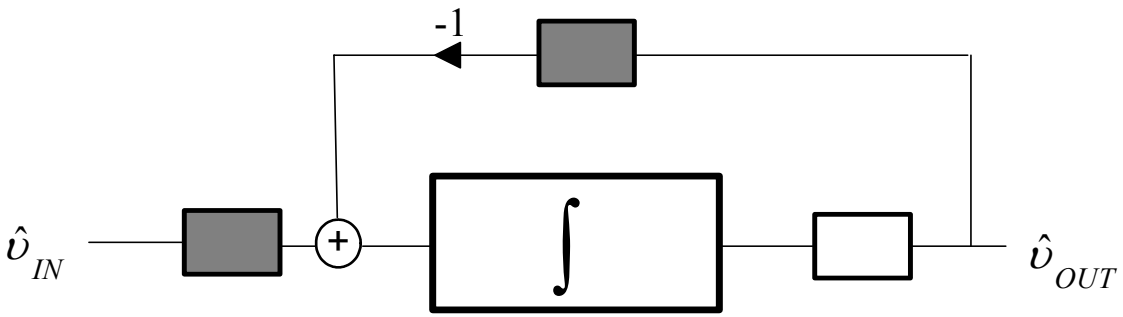
☹ The time constant is depended from temperature.

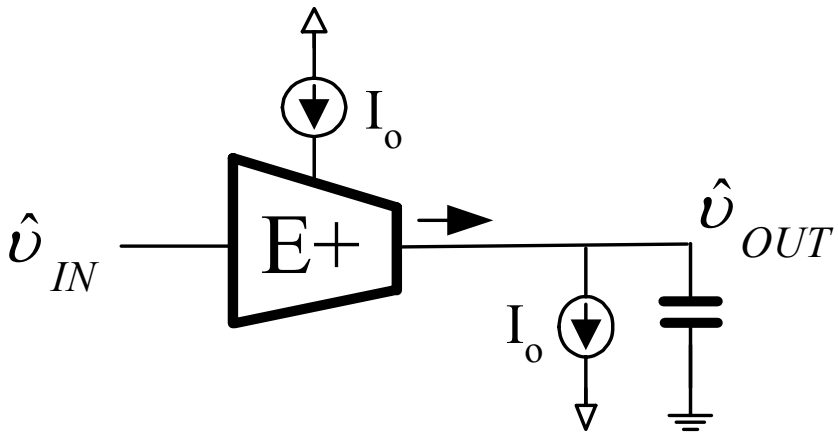
Lossless integrator-subractor



Lossy integrator

$$\tau \frac{d}{dt}\left[EXP\left(\hat{\upsilon}_{OUT}\right)\right] = EXP\left(\hat{\upsilon}_{IN}\right) - EXP\left(\hat{\upsilon}_{OUT}\right)$$



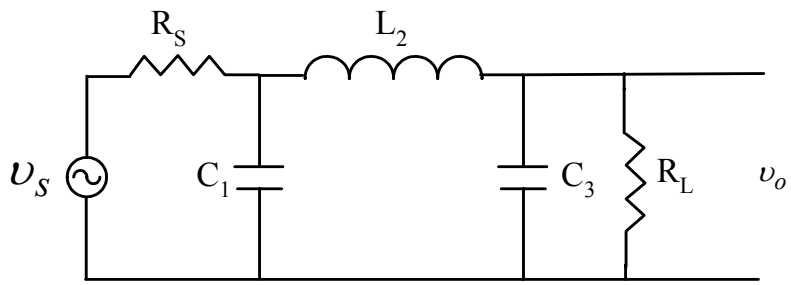


☺ Damping is achieved using a DC current source.

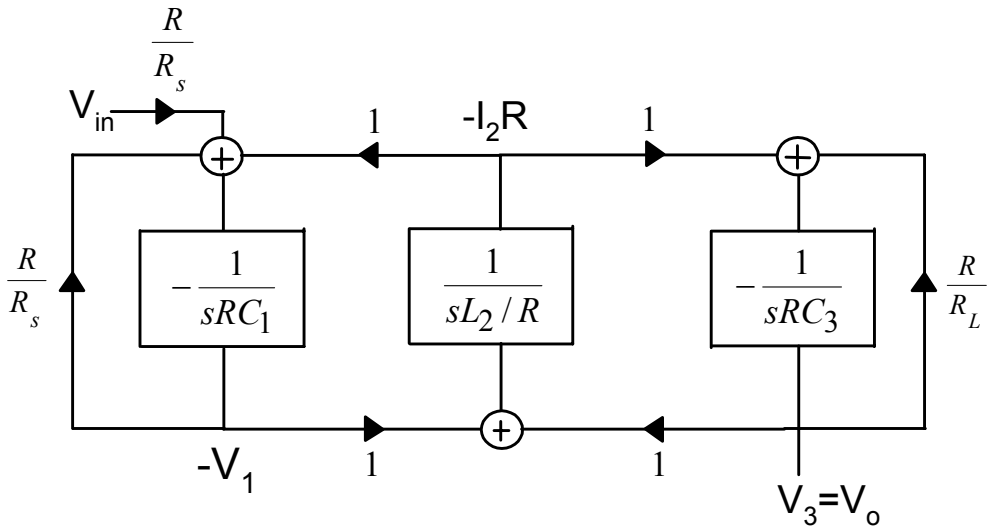
High-order Log-Domain filters

Operational simulation of all-pole LC ladders

✓ **LC ladder prototype**

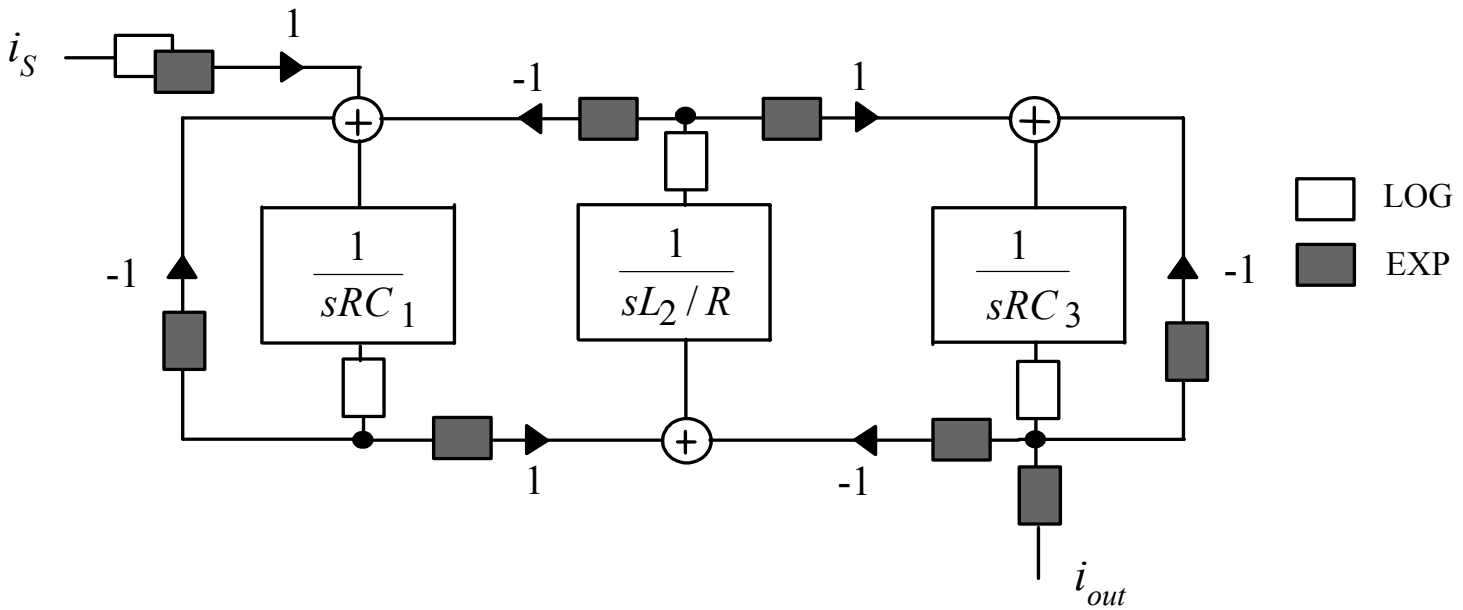


✓ **Linear domain Signal Flow Graph (SFG)**

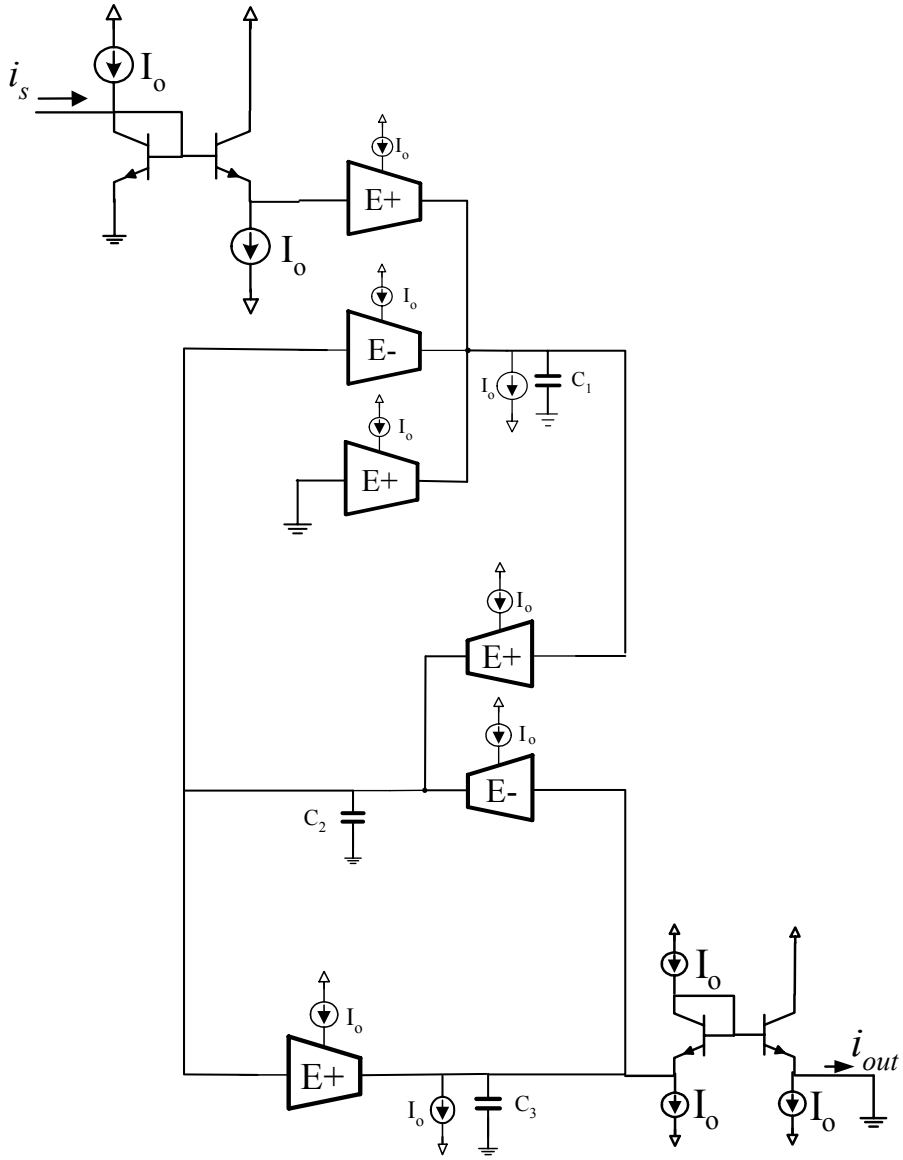


✓ Transposition to Log-Domain using the following rules:

- A LOG block is placed at the output of each integrator.
- An EXP block is placed at each input of integrators (before scaling).
- A LOG block is placed at the input of the system.
- An EXP block is placed at the output of the system.

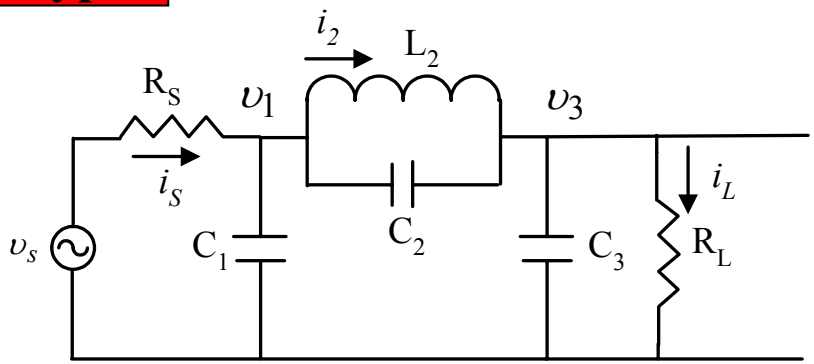


✓ **Implementation using Log-Domain cells**



Operational simulation LC ladders with finite zeros

✓ **LC ladder prototype**



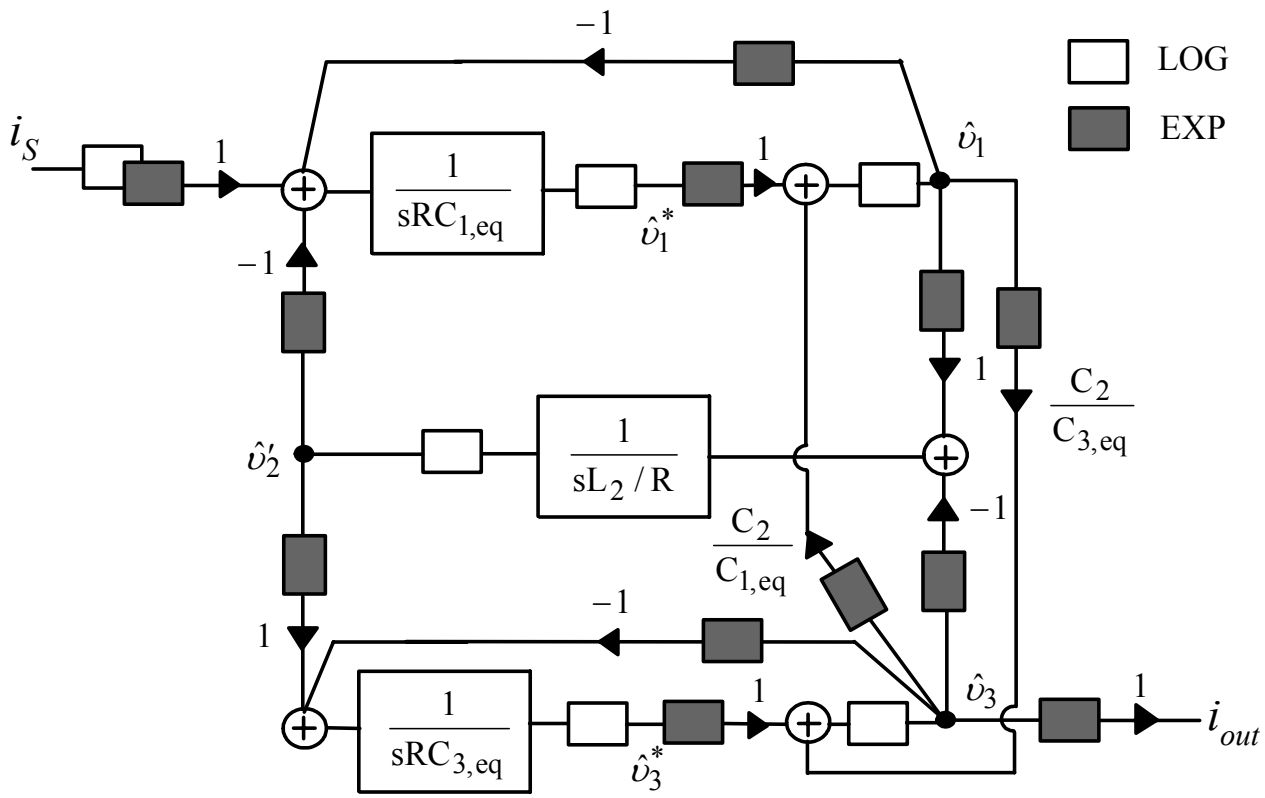
☹ Differentiation is required:

$$\upsilon_1 = \frac{1}{sRC_{1,eq}}(\upsilon'_S - \upsilon'_2 + sRC_2\upsilon_3)$$

☺ Alternative form without differentiation:

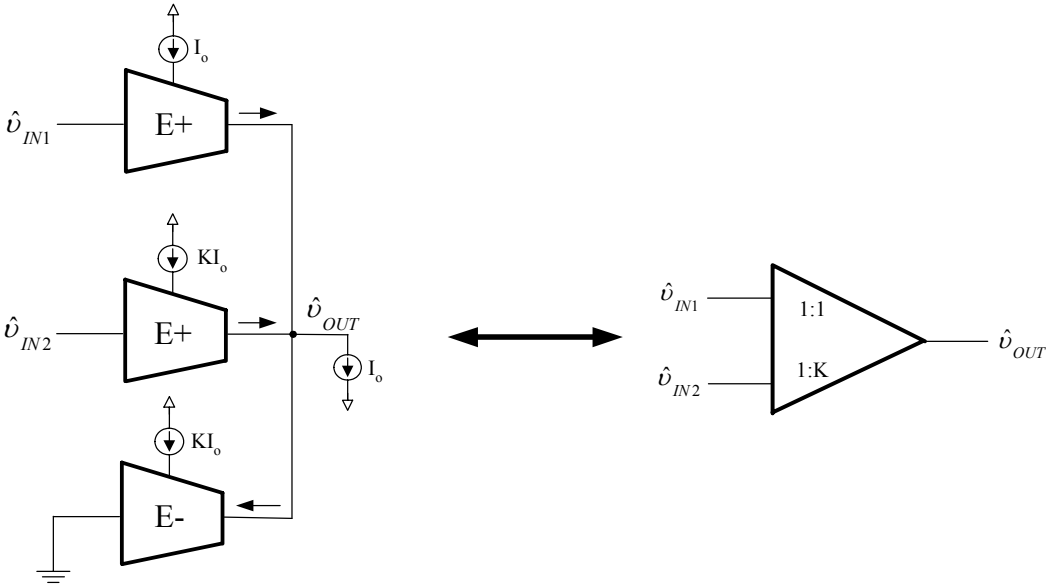
$$\upsilon_1 = \frac{1}{sRC_{1,eq}}(\upsilon'_S - \upsilon'_2) + \frac{C_2}{C_{1,eq}}\upsilon_3$$

✓ Log-Domain Signal Flow Graph (SFG)



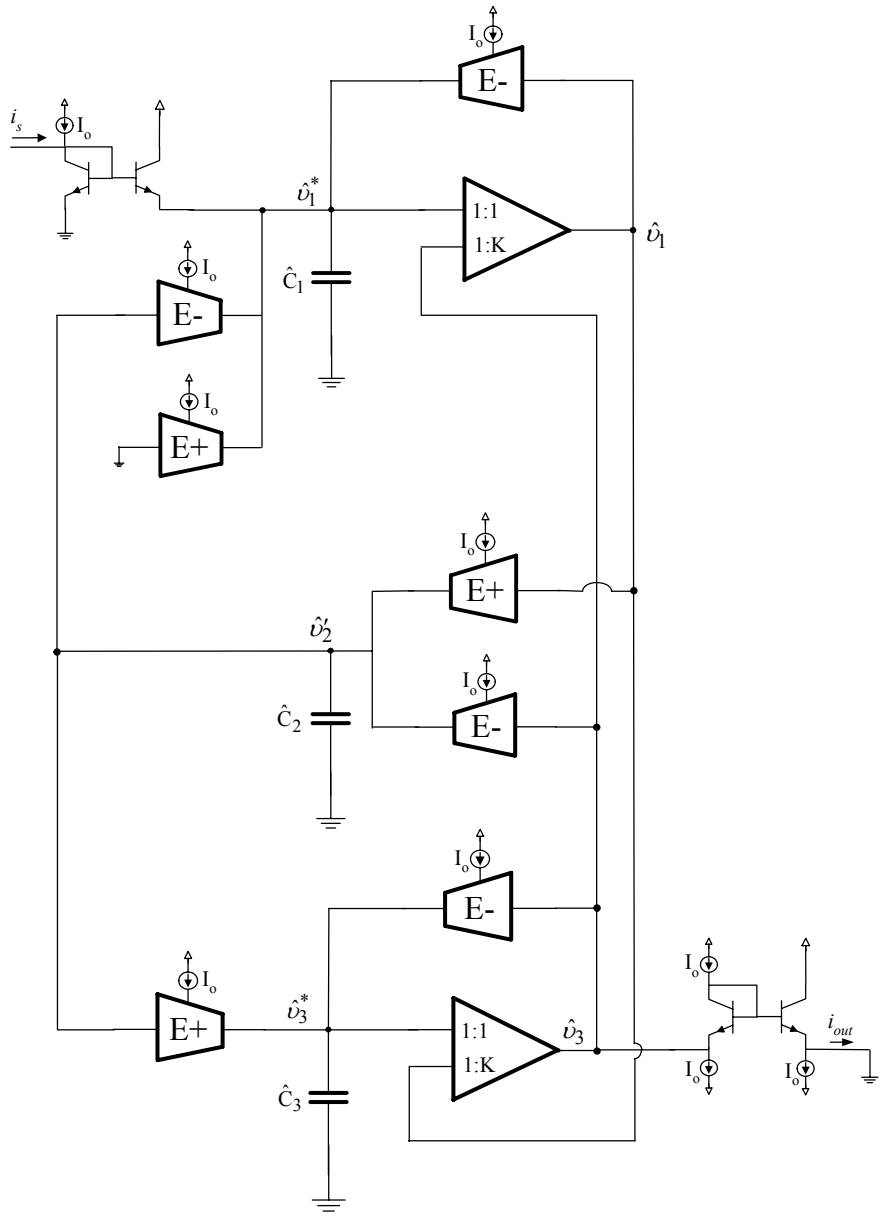
✓ Implementation using Log-Domain cells

Log-Domain summing block

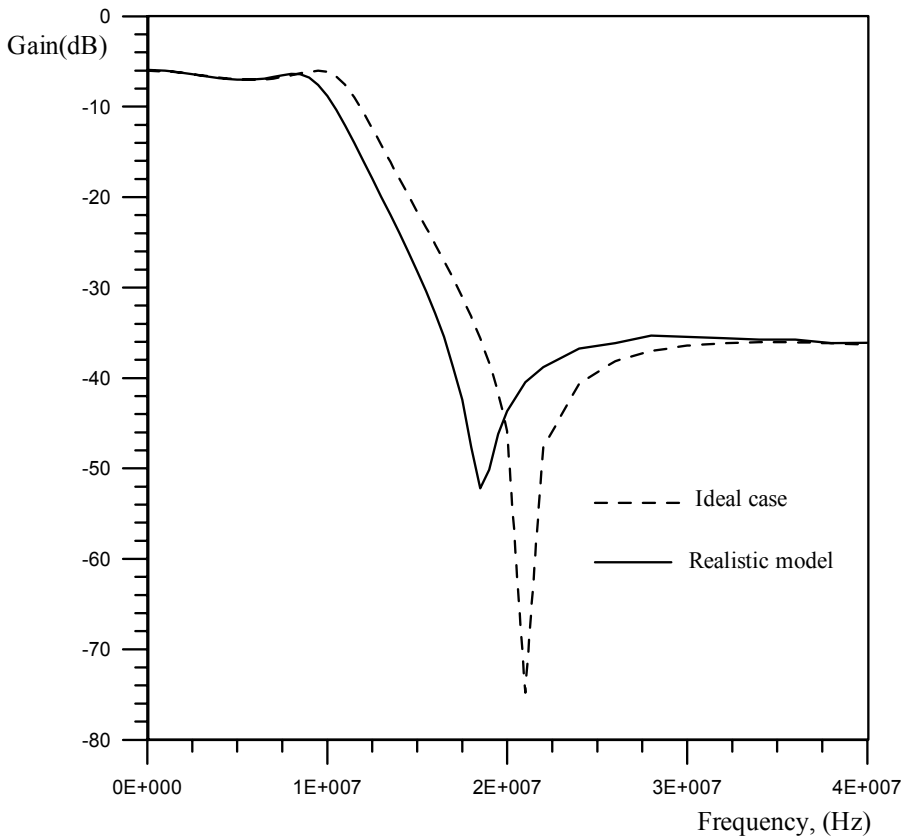


$$EXP(\hat{\upsilon}_{out}) = EXP(\hat{\upsilon}_1) + K \cdot EXP(\hat{\upsilon}_2)$$

Log-Domain elliptic filter



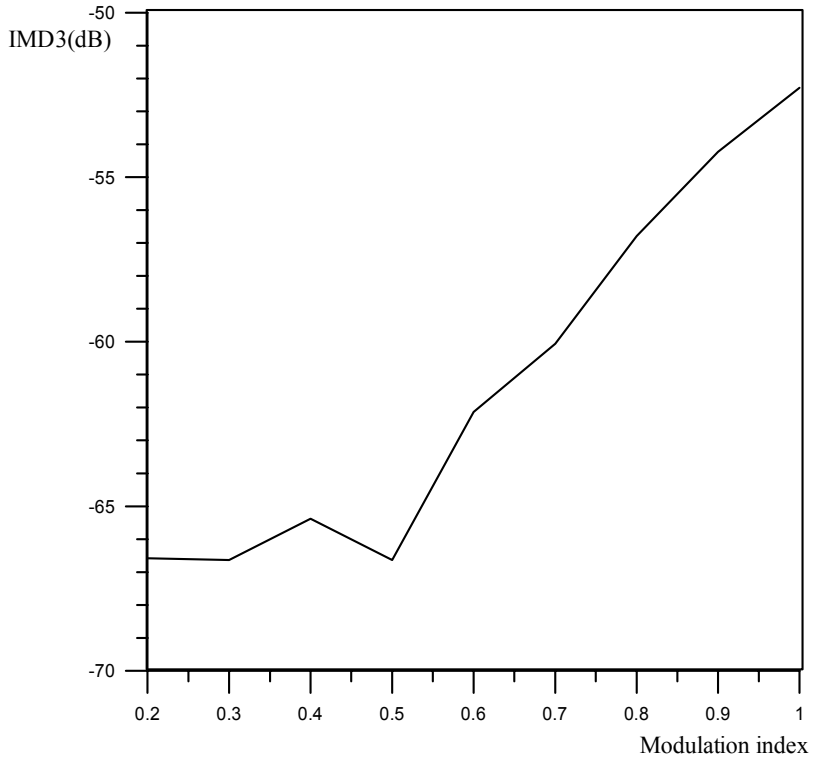
Frequency response of the filter @ modulation index factor 0.8



☑ The frequency response of a Log-Domain filter is evaluated using large-signal transient simulations and FFT analysis.

☹ The AC analysis of HSPICE is valid only for small modulation index factor !!!

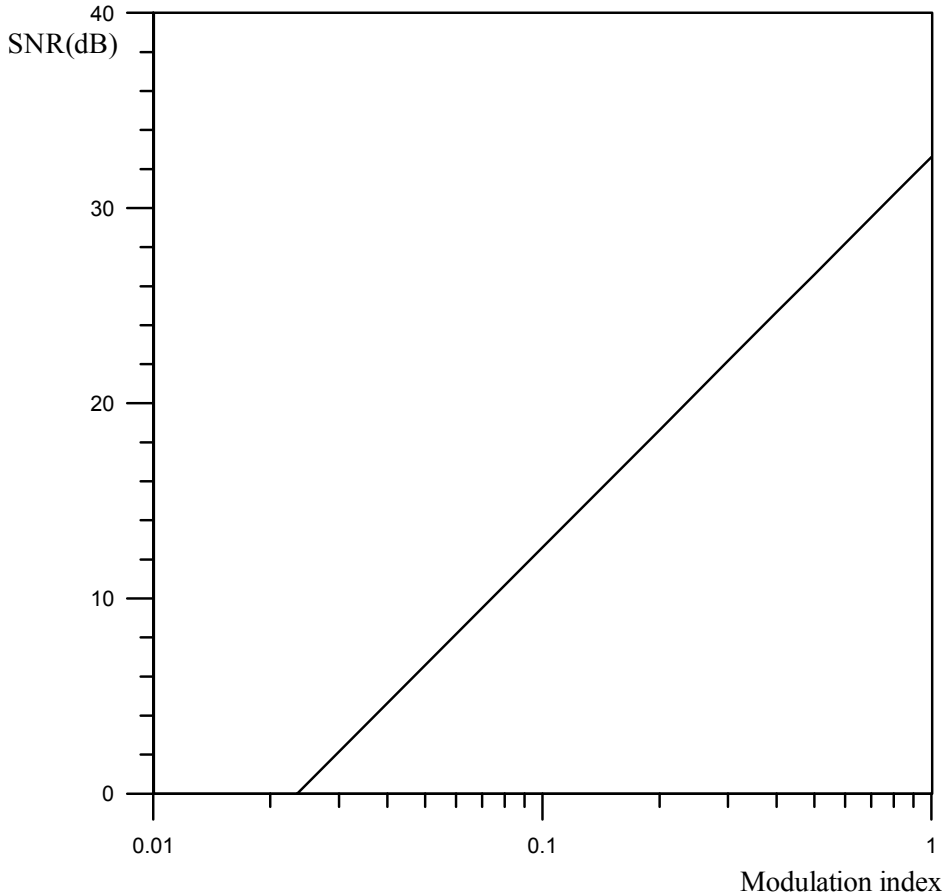
Non-linear analysis



☑ A two-tone test was performed, in order to measure the third-order intermodulation distortion factor.

☺ The IMD3 was -52dB @ modulation index equal to 1.

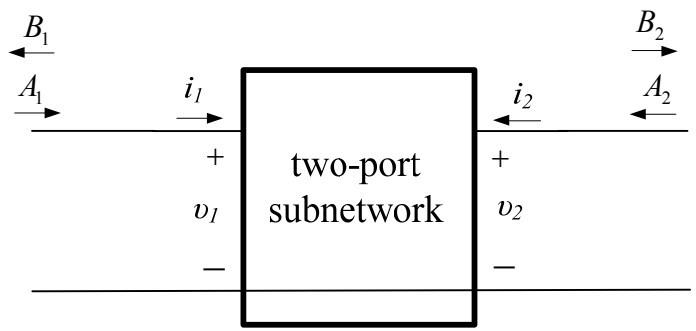
Noise analysis



☺ The achieved Dynamic Range was 35dB.

Log-Domain Wave filters

Wave variables

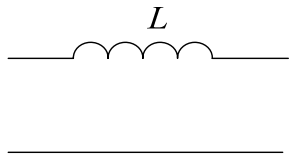


incident wave $$A_k = i_k + \frac{v_k}{R} \qquad (k = 1,2)$$

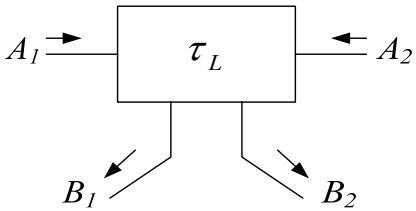
reflected wave $$B_k = i_k - \frac{v_k}{R} \qquad (k = 1,2)$$

Scattering parameters description

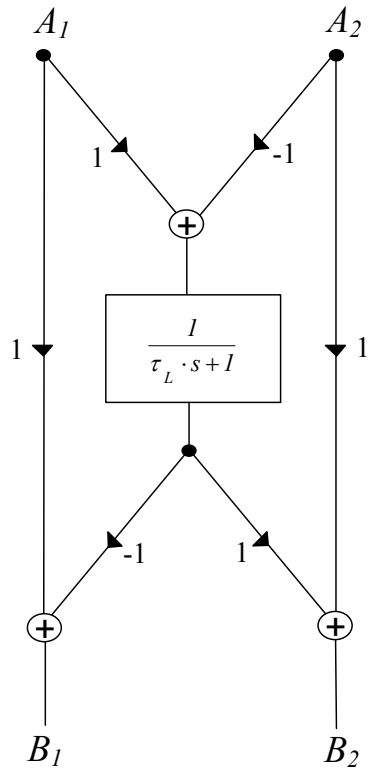
Passive element



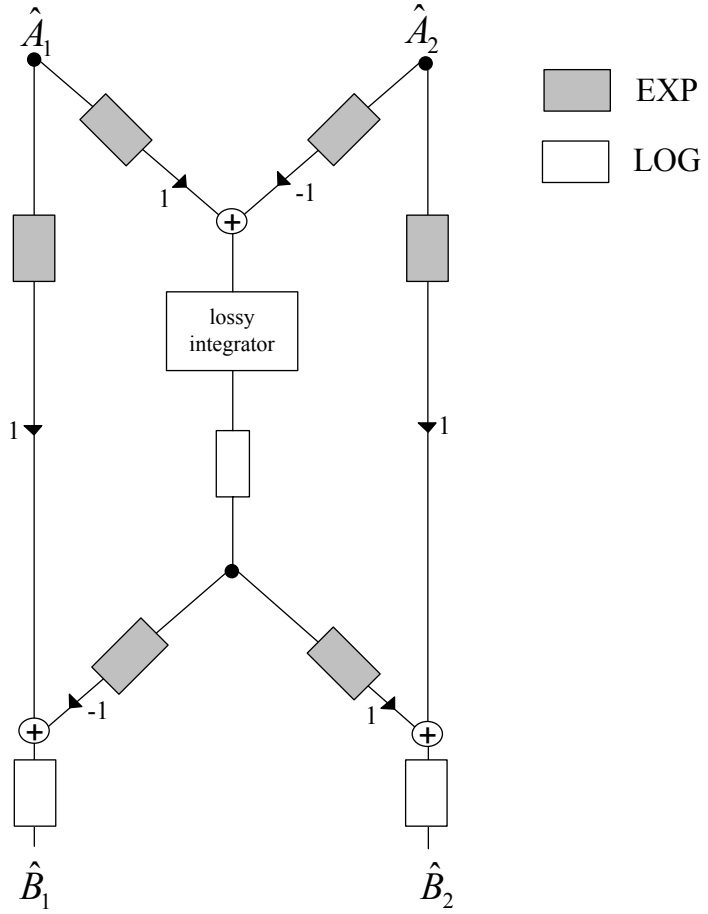
Symbol of wave equivalent in the log-domain

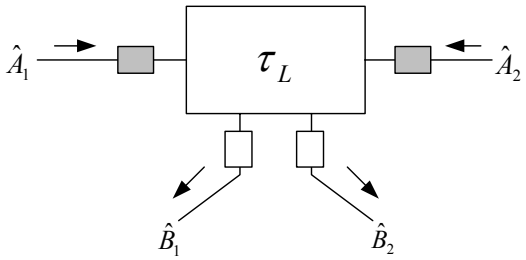


$$\begin{bmatrix} B1 \\ B2 \end{bmatrix} = \frac{1}{1+\tau_L s}\begin{bmatrix} \tau_L \cdot s & 1 \\ 1 & \tau_L \cdot s \end{bmatrix} \cdot \begin{bmatrix} A1 \\ A2 \end{bmatrix}$$

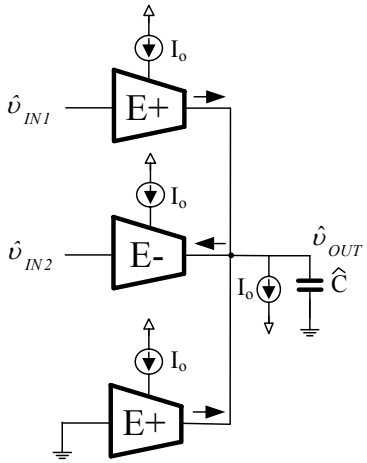


✓ Transposition of linear domain SFG to the Log-Domain SFG

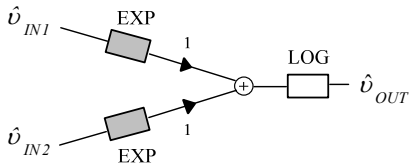


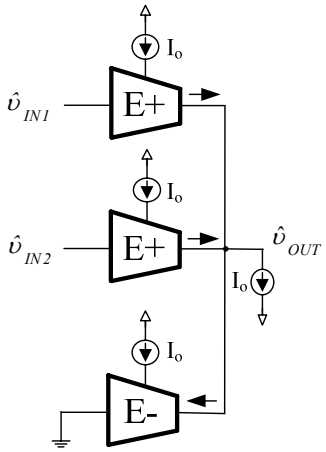


Lossy integration

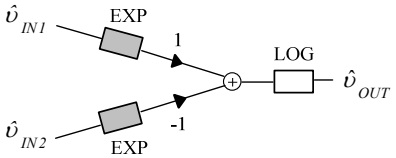


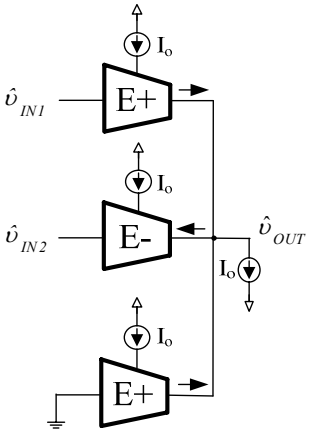
Summation



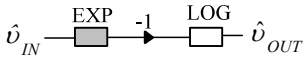


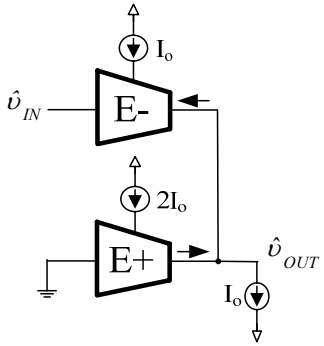
Subtraction



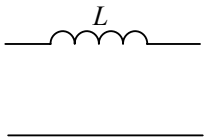
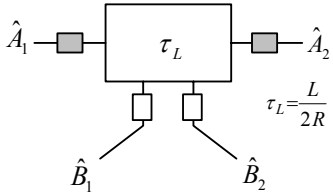
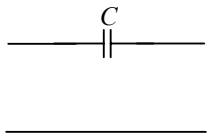
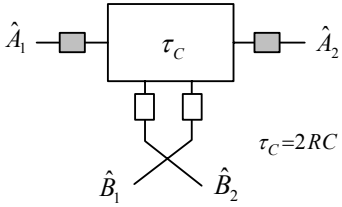
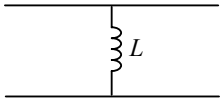
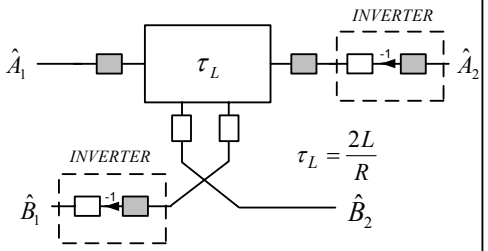
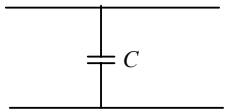
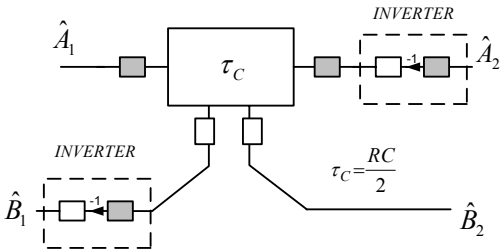


Inversion

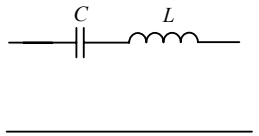
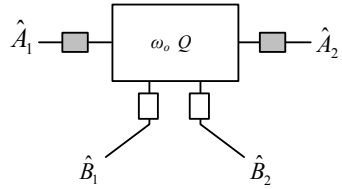
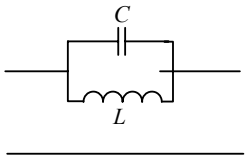
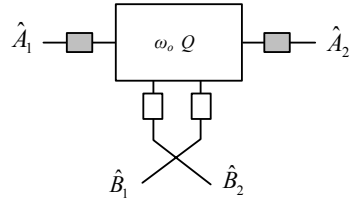
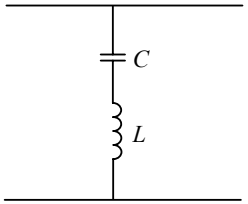
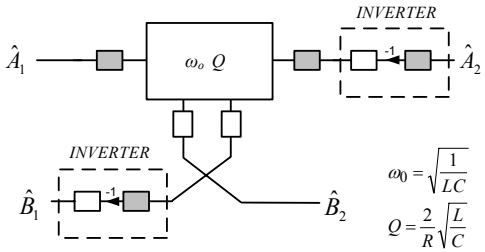
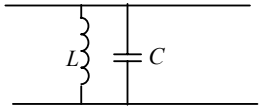
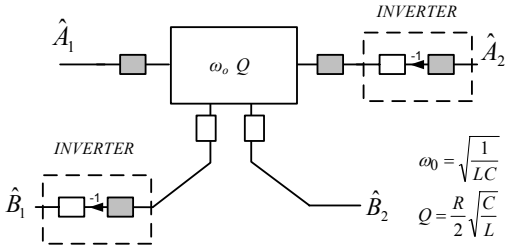




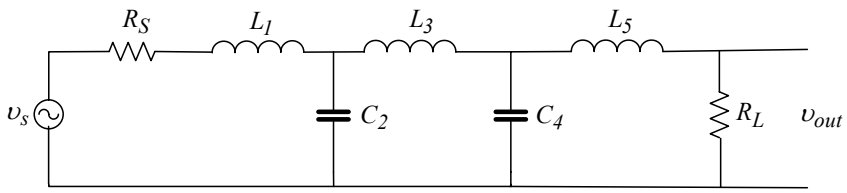
✓Log-domain wave equivalents of 1st-order blocks

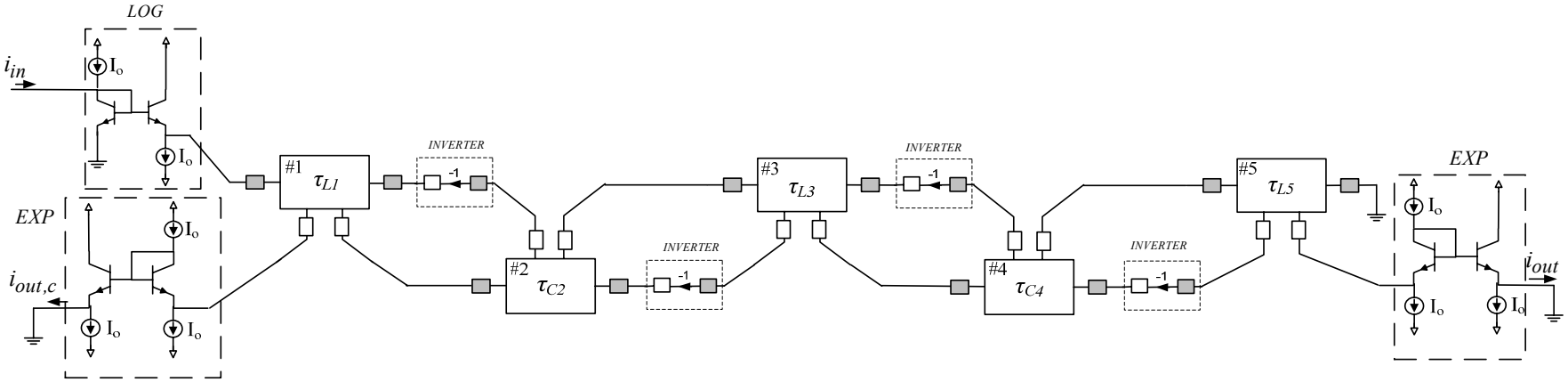
Prototype	Log-Domain wave equivalent
	
	
	
	

✓Log-domain wave equivalents of 2nd-order blocks

Prototype	Log-Domain wave equivalent
	 $\omega_0 = \sqrt{\frac{1}{LC}}$ $Q = \frac{1}{2R}\sqrt{\frac{L}{C}}$
	 $\omega_0 = \sqrt{\frac{1}{LC}}$ $Q = 2R\sqrt{\frac{C}{L}}$
	 $\omega_0 = \sqrt{\frac{1}{LC}}$ $Q = \frac{2}{R}\sqrt{\frac{L}{C}}$
	 $\omega_0 = \sqrt{\frac{1}{LC}}$ $Q = \frac{R}{2}\sqrt{\frac{C}{L}}$

Log-Domain wave filter





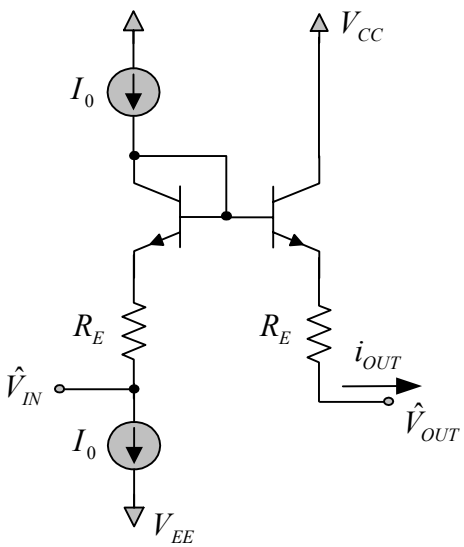
☺ A quick design procedure is offered.

☺ Modular filter structures are derived.

☹ The circuit complexity is increased in comparison to the leapfrog filters.

Effects of non-idealities

✓ **Effect of non-zero R_E**

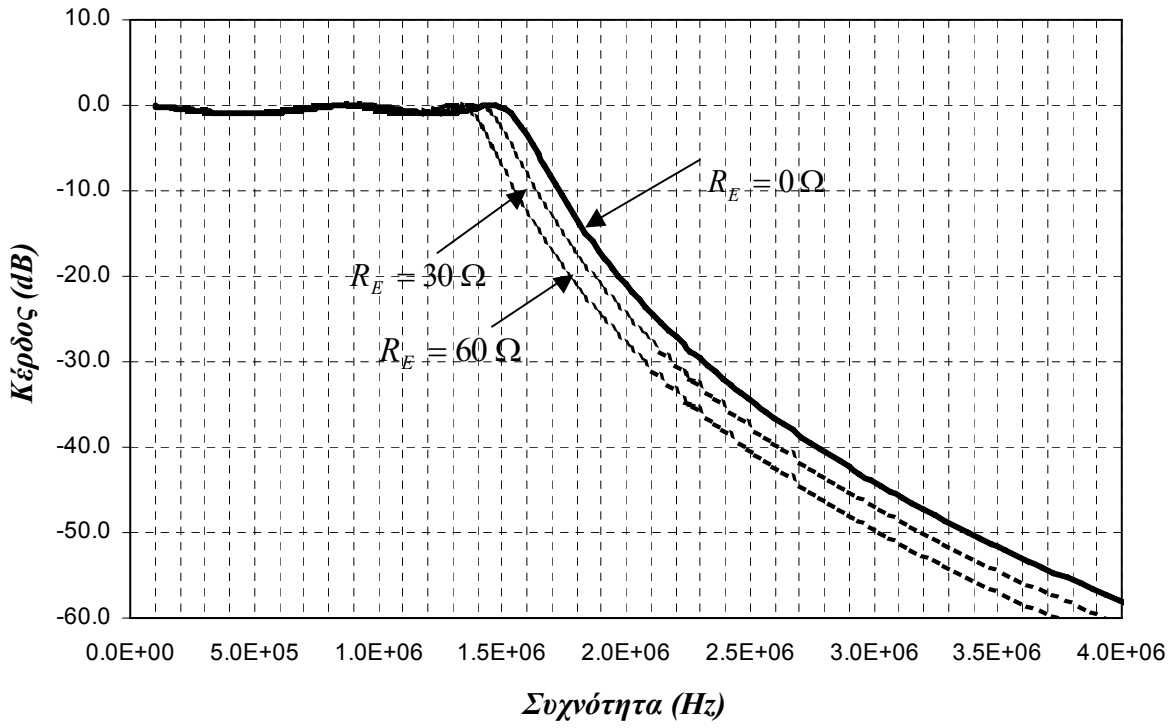


$$I_{OUT} = I_0 e^{\frac{\hat{\upsilon}_{IN} - \hat{\upsilon}_{OUT}}{V_T + \frac{R_B}{\beta} I_0}}$$

☹ The cut-off frequency is shifted, while the filter shape remains unchanged.

- Input-output relationship for a lossy integrator

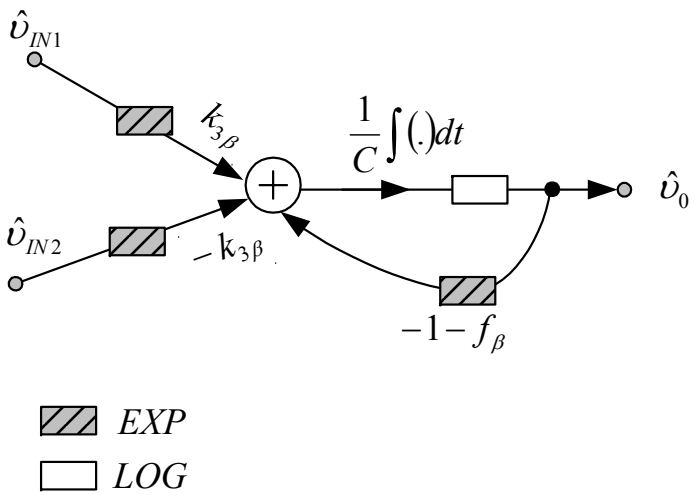
$$\frac{\left(V_T + I_0 R_E\right)}{V_T}\frac{\hat{C}V_T}{I_0}\frac{d}{dt}\left[EXP\left(\hat{\upsilon}_1\right)\right] = \int EXP\left(\hat{A}_1\right) - EXP\left(\hat{A}_2\right) + EXP\left(\hat{\upsilon}_1\right)$$



☺ The effect of non-zero R_E is compensated by multiplying the value of DC current source by a factor

$$k_{RE} = \frac{\left(V_T + I_0 R_E\right)}{V_T}$$

✓ Effect of BJT transistor finite beta.

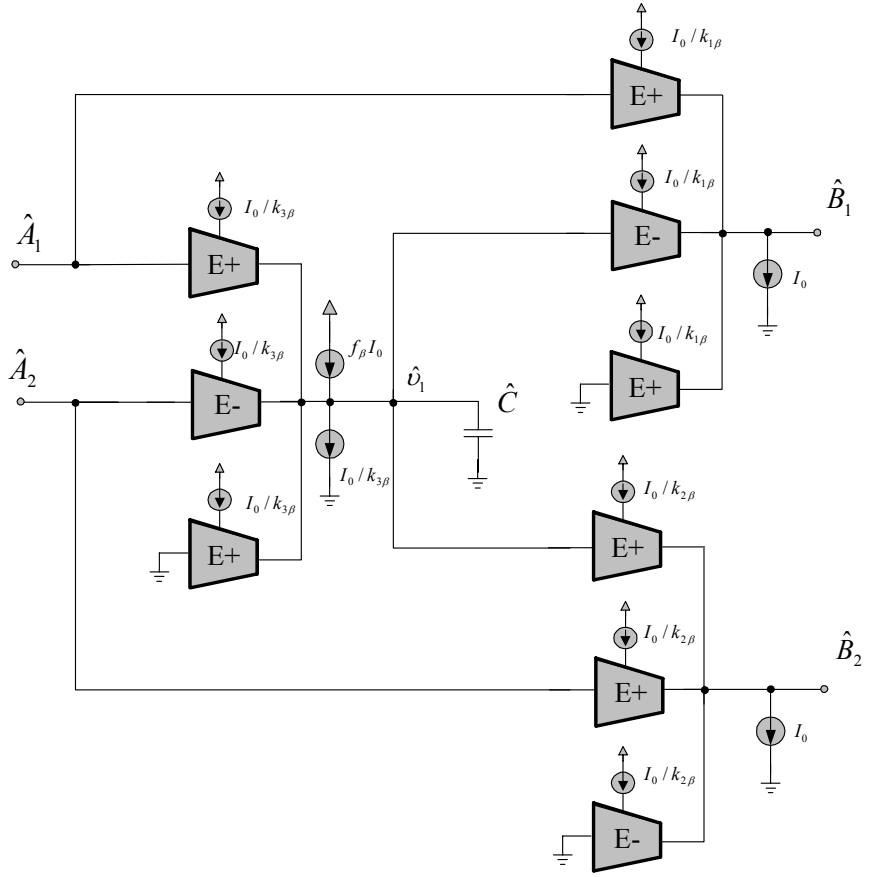


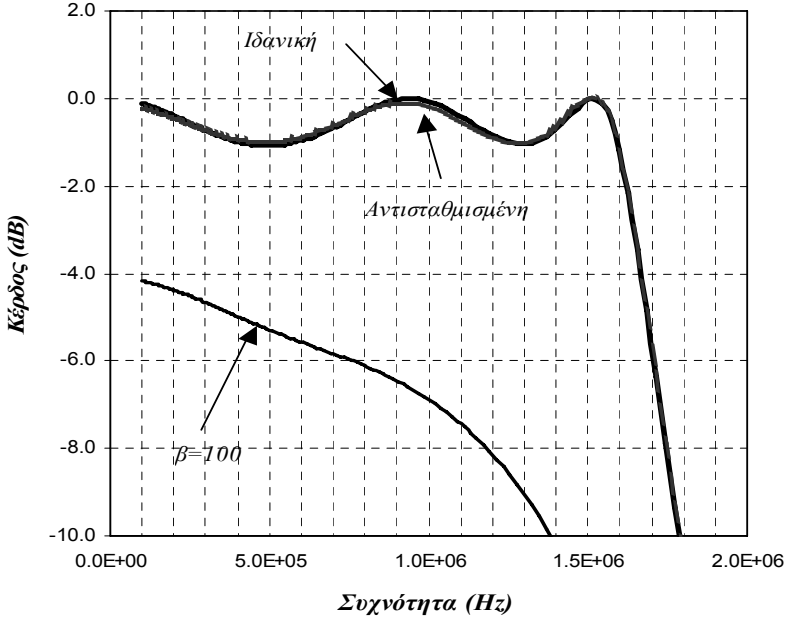
☹ **The finite beta introduces a scalar error and an extra feedback path.**

☹ **The cut-off frequency and the phase response of the filter are changed.**

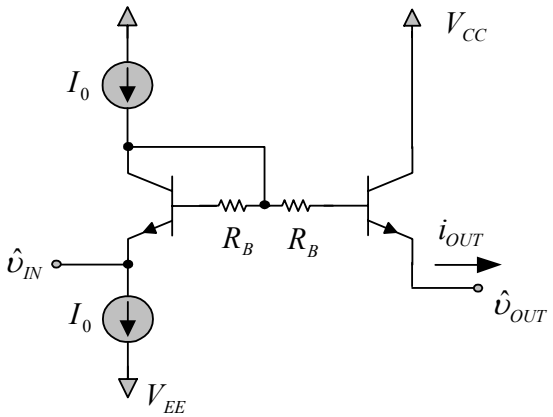
☺ **The above imperfections can be electronically removed.**

▪Wave equivalent of a floating inductance, with additional circuitry for removing the effect of finite beta.

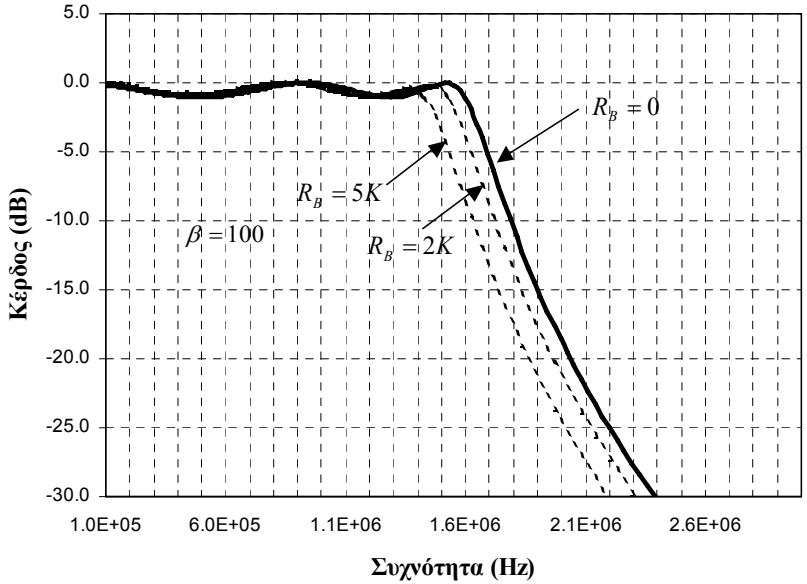




✓ **Effect of non-zero R_B.**



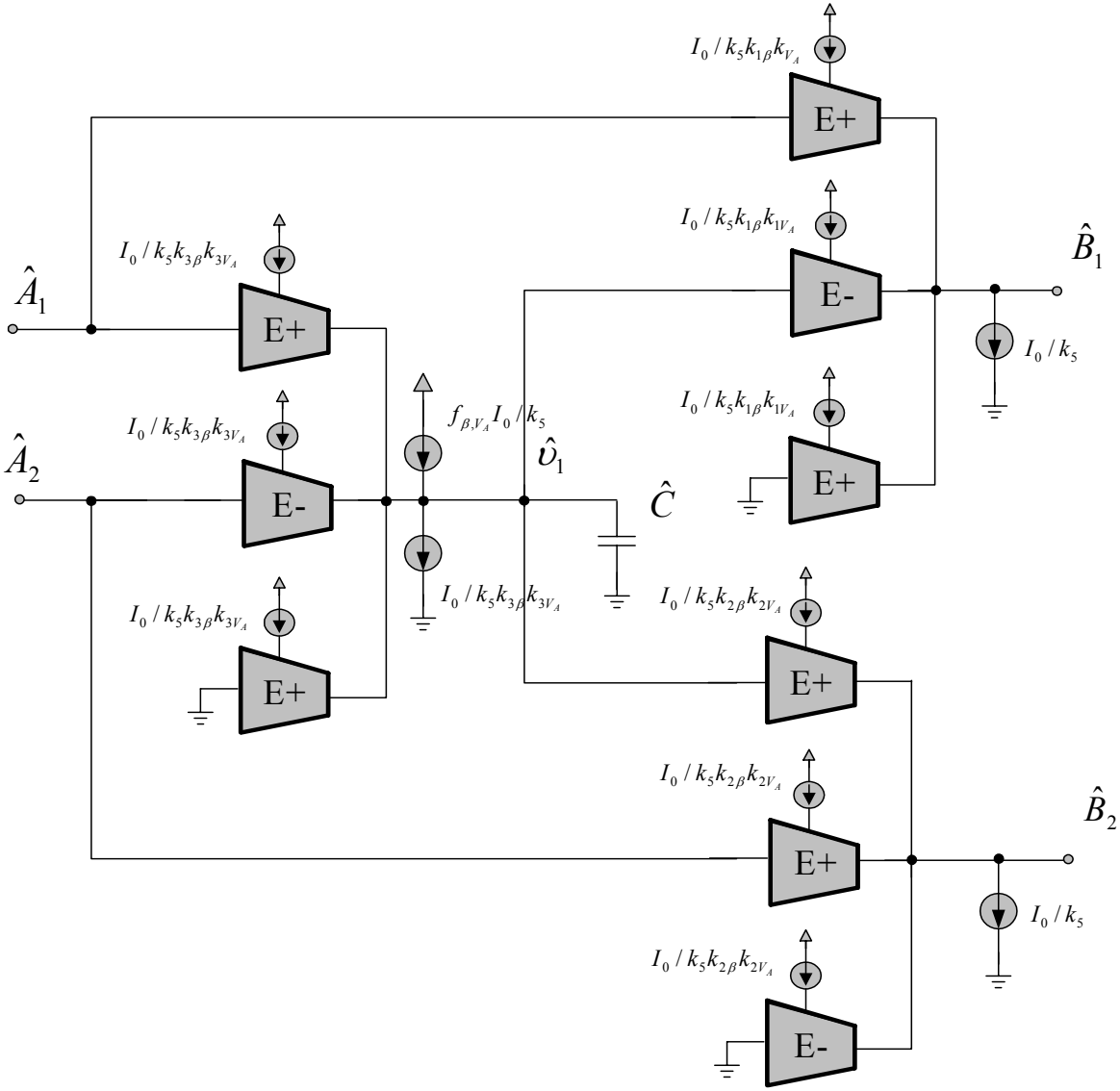
$$I_{OUT} = I_0 e^{\frac{\hat{\upsilon}_{IN} - \hat{\upsilon}_{OUT}}{V_T + \frac{R_B}{\beta} I_0}}$$



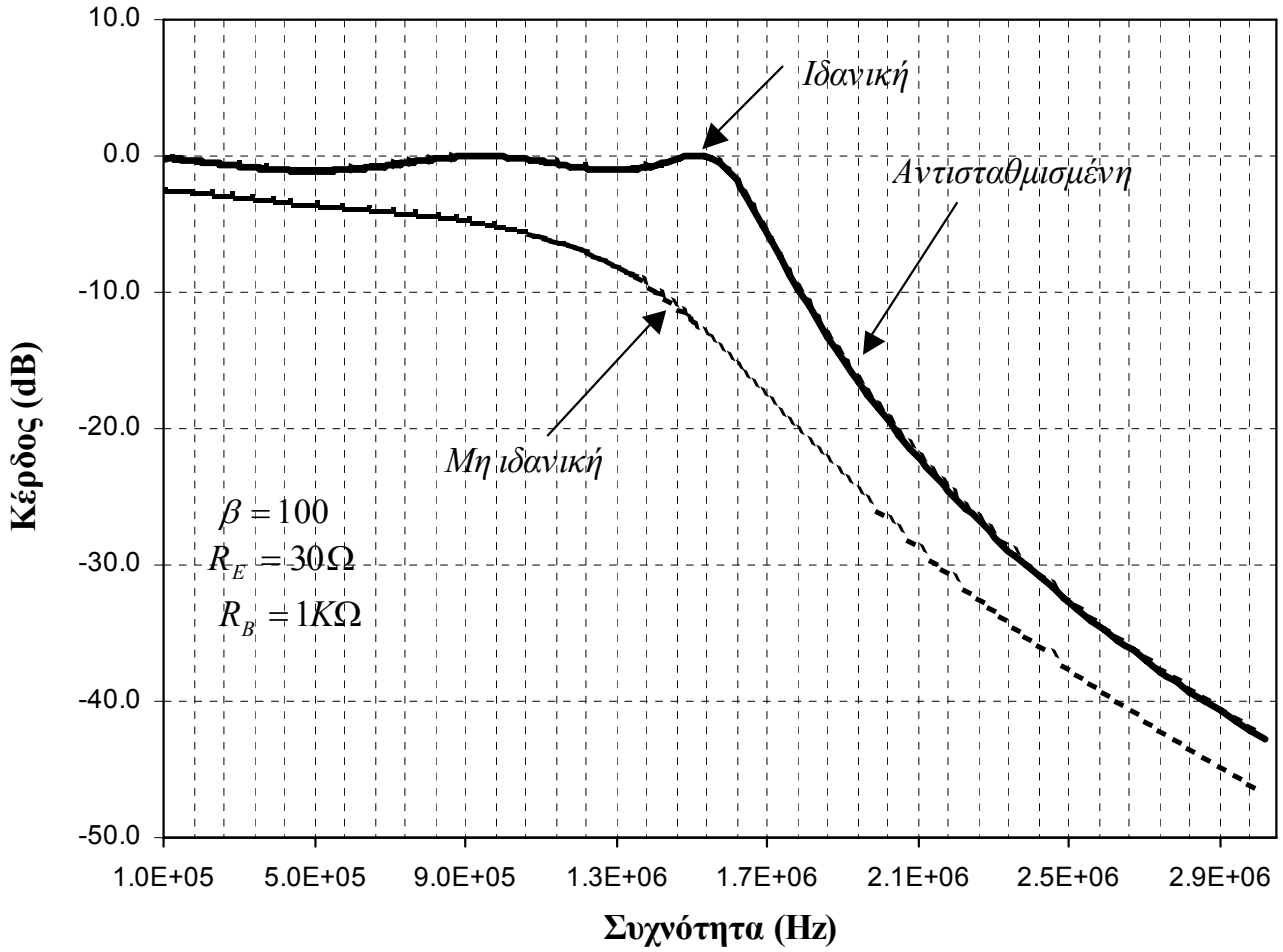
☹ The cut-off frequency is shifted, while the filter shape remains unchanged.

☺ This deviation is canceled by following the same procedure as in non- zero R_E.

✓ Combined effects



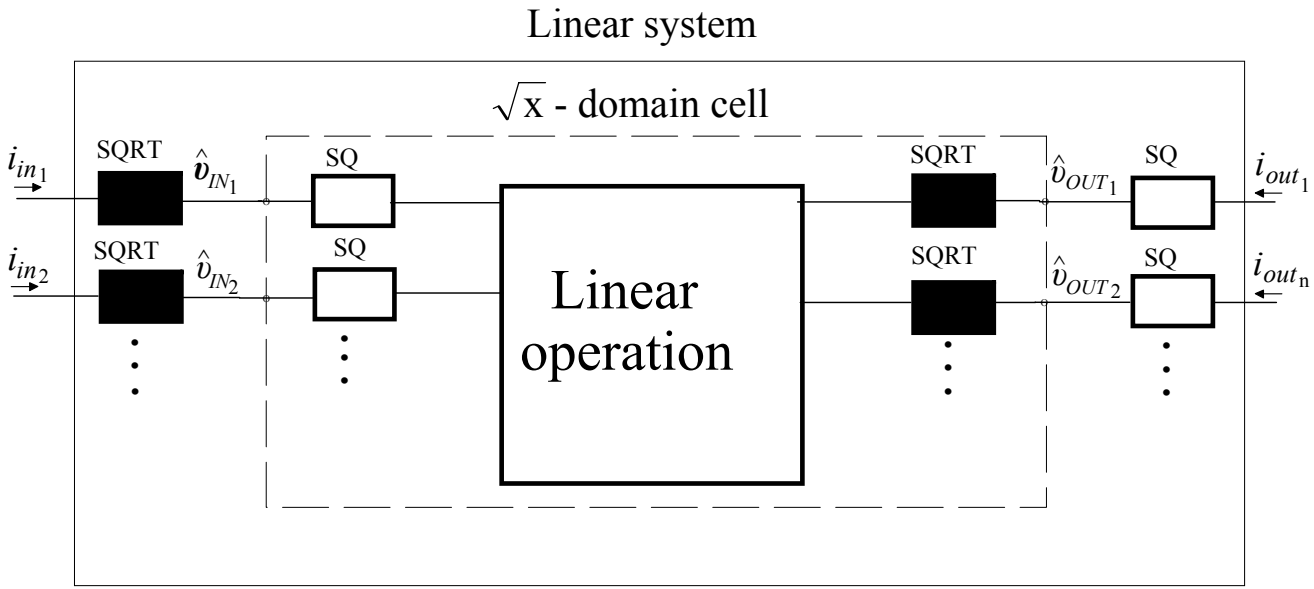
- The values of factors are calculated using a fitting algorithm.



Square-Root-Domain filters

A method for designing Square-Root-Domain filters

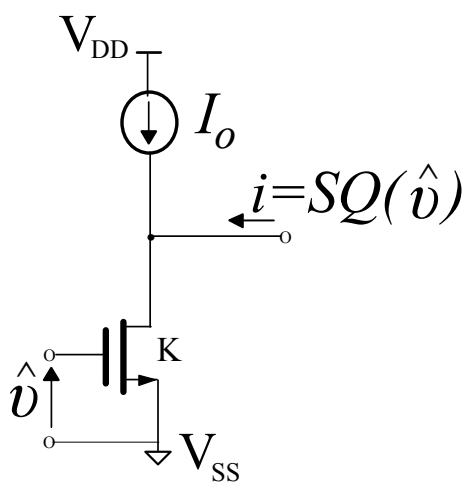
✓ **Representation of a Square-Root-Domain filter using complementary operators**

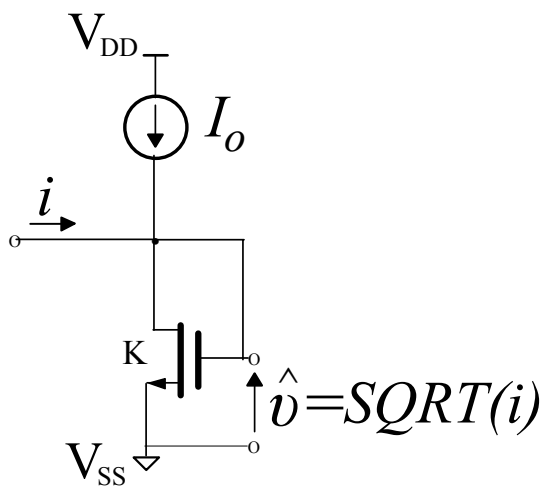


- **Definition of operators**

$$SQ(\hat{\upsilon}) = \frac{K}{2}\left(\hat{\upsilon} - V_T\right)^2 - I_o \qquad SQRT(i) = \sqrt{\frac{2(i + I_O)}{K}} + V_T$$

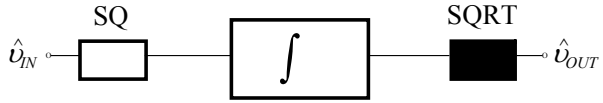
$$SQ[SQRT(i)] = i$$

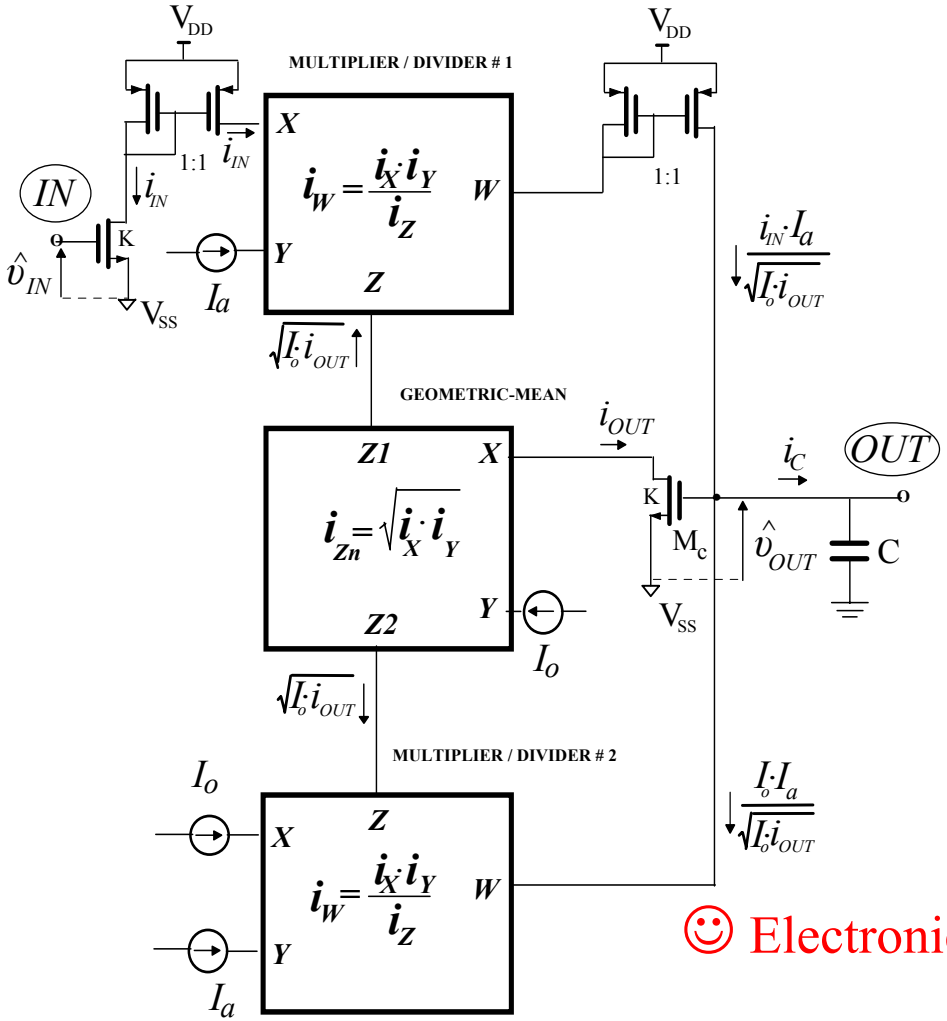




Square-Root-Domain integrators

Lossless integrator





$$i_c = C\frac{d\hat{\upsilon}_{OUT}}{dt} = \frac{i_{IN} I_a}{\sqrt{I_o i_{OUT}}} - \frac{I_o I_a}{\sqrt{I_o i_{OUT}}}$$

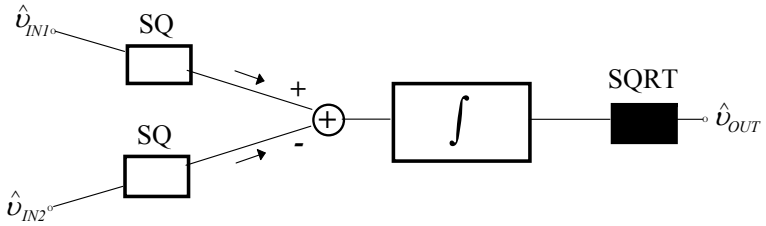
$$SQ(\hat{\upsilon}_{OUT}) = \frac{1}{\tau}\int SQ(\hat{\upsilon}_{IN}) \cdot dt$$

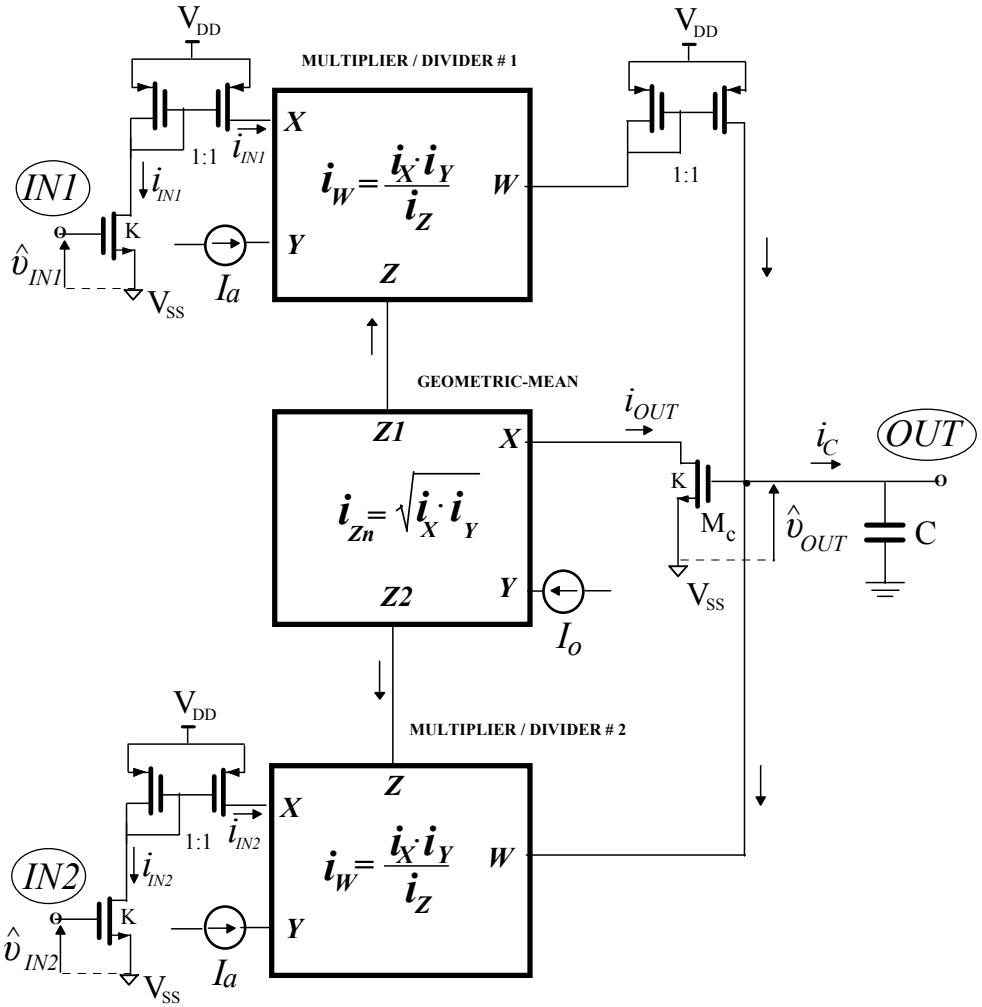
The time-constant of integrator is:

$$\tau = \frac{C\sqrt{I_o}}{\sqrt{2K}\, I_a}$$

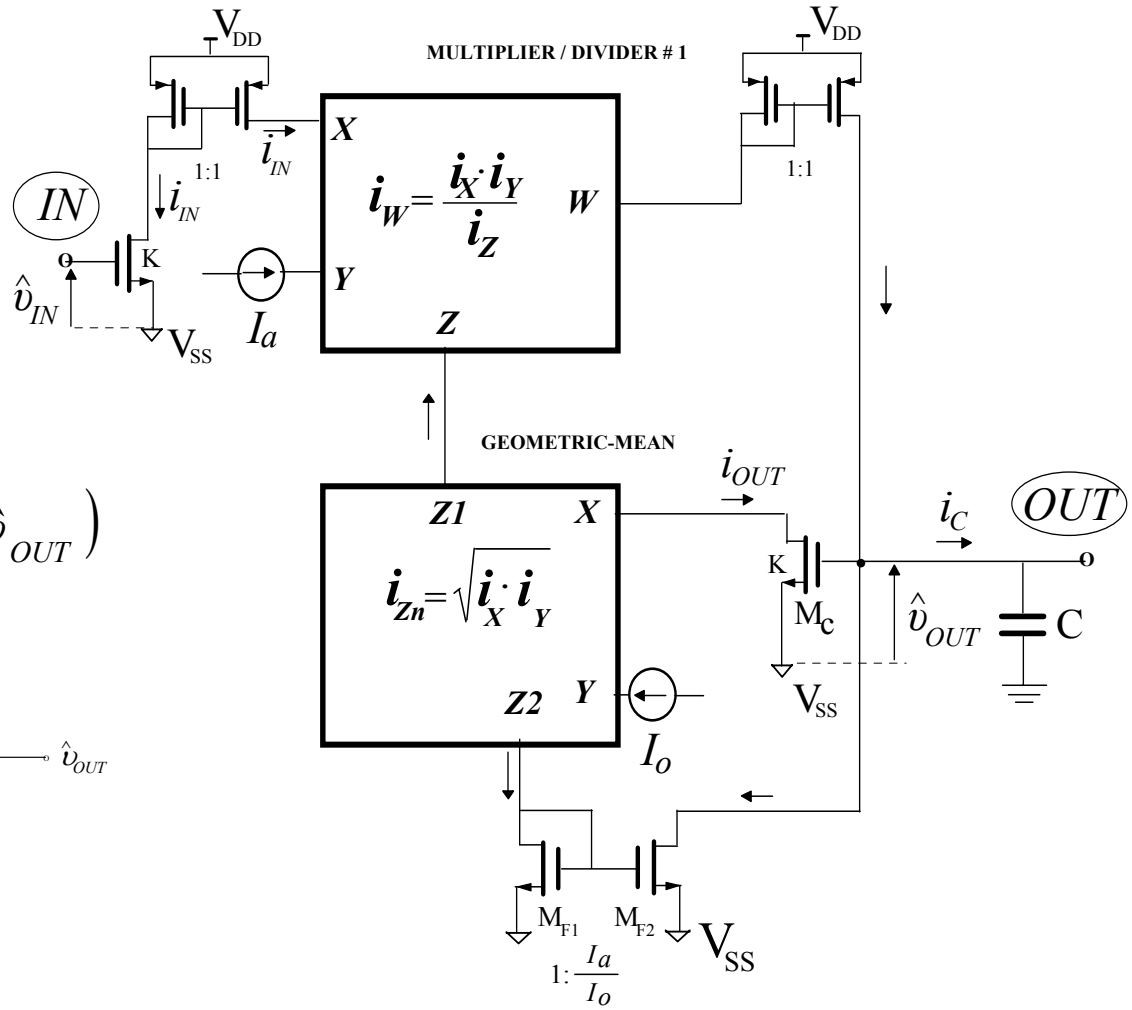
☺ Electronic tuneability using a DC current source.

Lossless integrator-subtractor

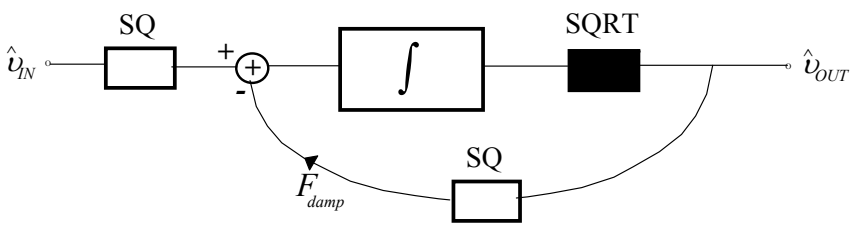




Lossy integrator

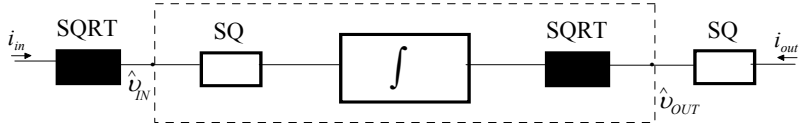


$$\tau \frac{d}{dt}\left[SQ\left(\hat{\upsilon}_{OUT}\right)\right] = SQ\left(\hat{\upsilon}_{IN}\right) - F_{damp}\, SQ\left(\hat{\upsilon}_{OUT}\right)$$

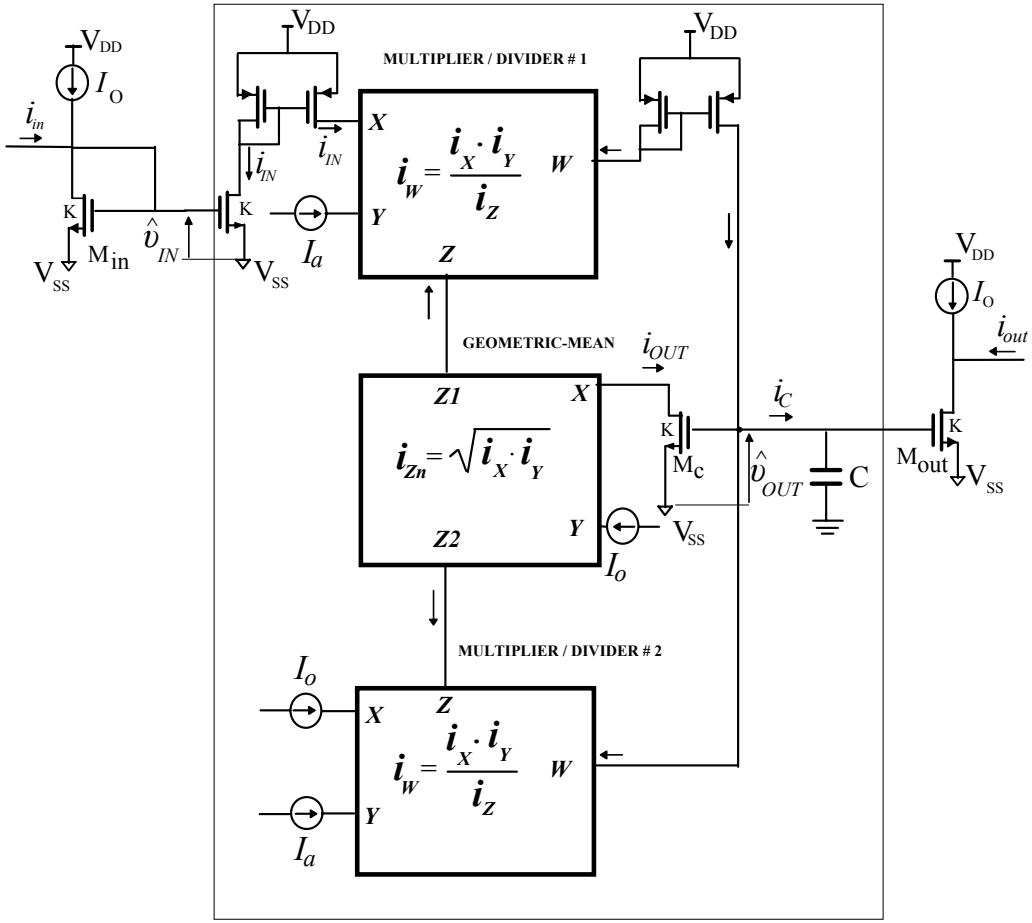


☺ Damping is achieved using a current mirror.

Complete system of current integrator

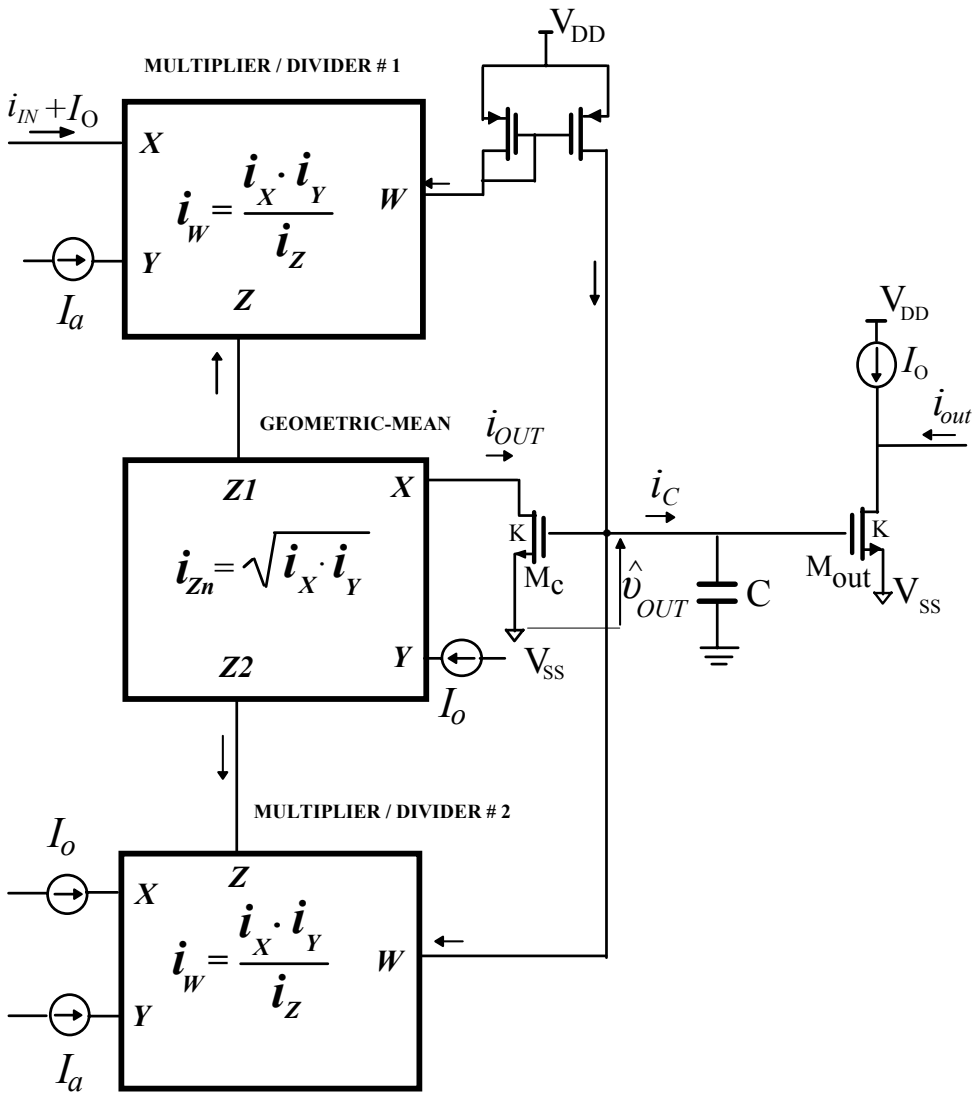


$\sqrt{x}$ - domain cell

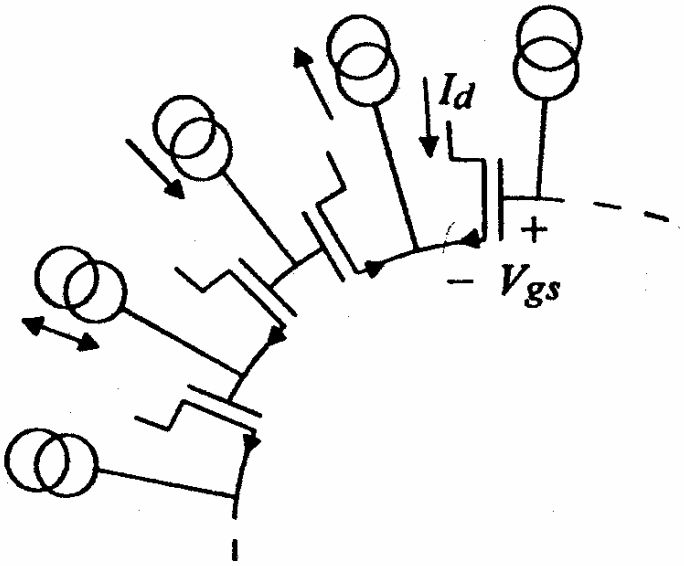


$\sqrt{x}$ - domain cell

Simplification of circuit:



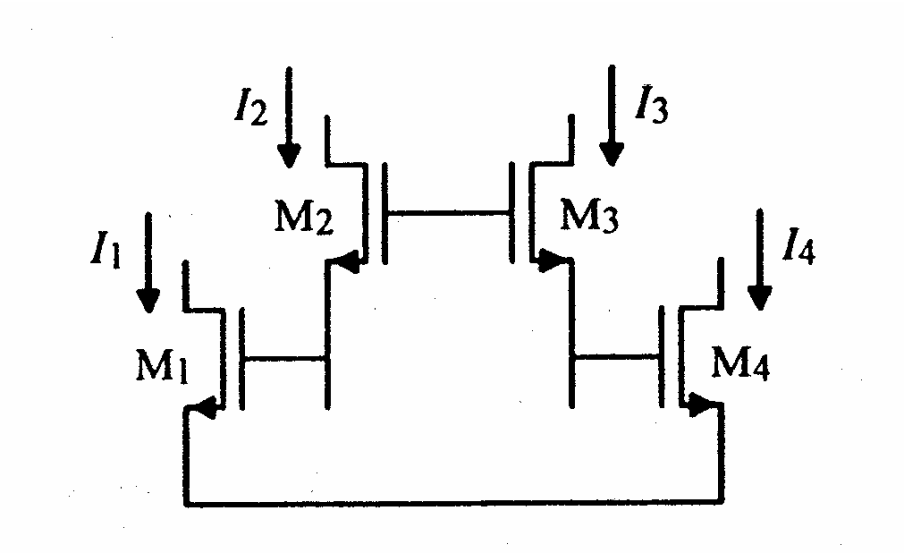
MOS Translinear principle



✓In the closed loop, the gate-source voltages are in series, with equal number of transistors arranged clockwise and counter-clockwise.

$$\sum_{cw}\sqrt{\frac{I_D}{W/L}} = \sum_{ccw}\sqrt{\frac{I_D}{W/L}}$$

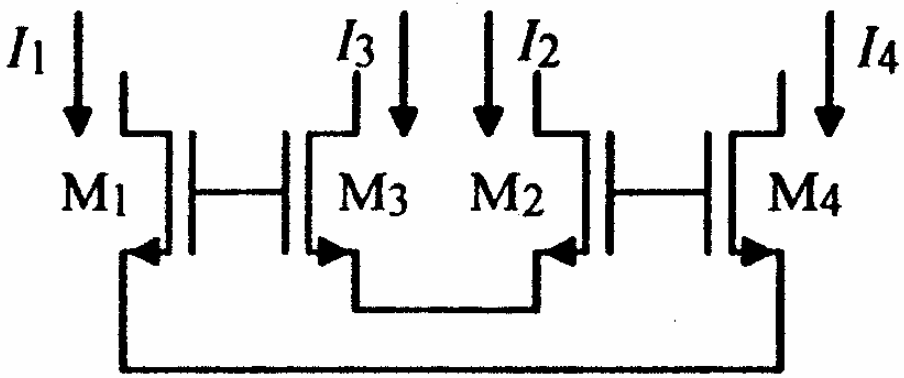
Stacked topology



☺ Offers simple circuits.

☹ Suffers from a strong influence of the body effect.

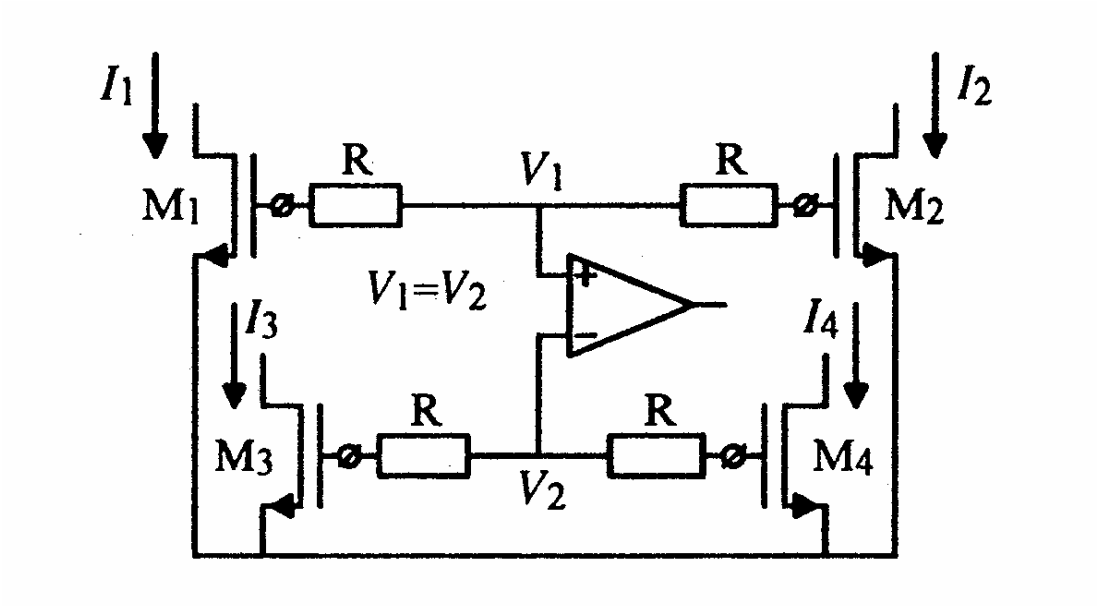
Up-down topology



☺ The body effect is much smaller than that in case of stacked topology.

☹ Requires some extra circuitry, in comparison with the stacked configuration.

Electronically simulated loop topology



✓ The average of the gate-source voltages of transistors M_1 and M_2 is forced equal to the average of the gate-source voltages of transistors M_3 and M_4.

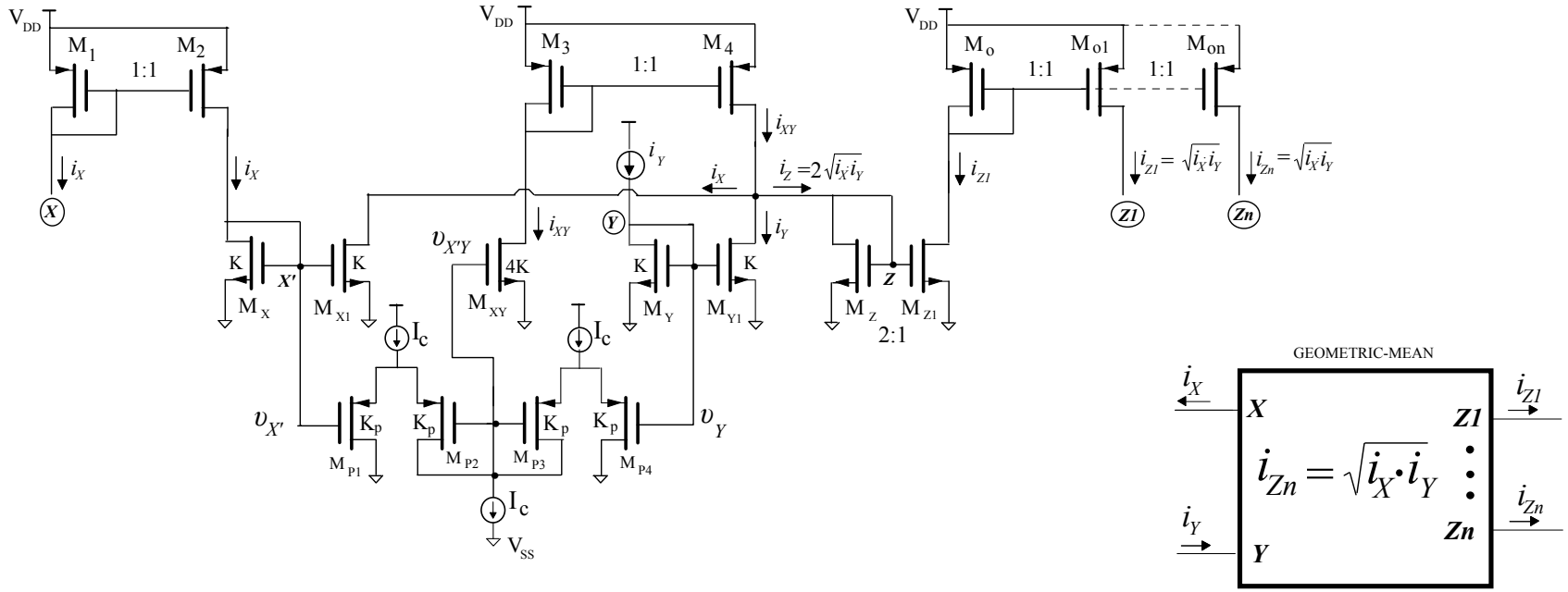
☺ The body effect is completely eliminated.

☹ The achieved bandwidth is limited by the speed of additional circuitry.

☹ A relative large number of elements is required in same cases.

Basic SQRD blocks

Current geometric-mean circuit

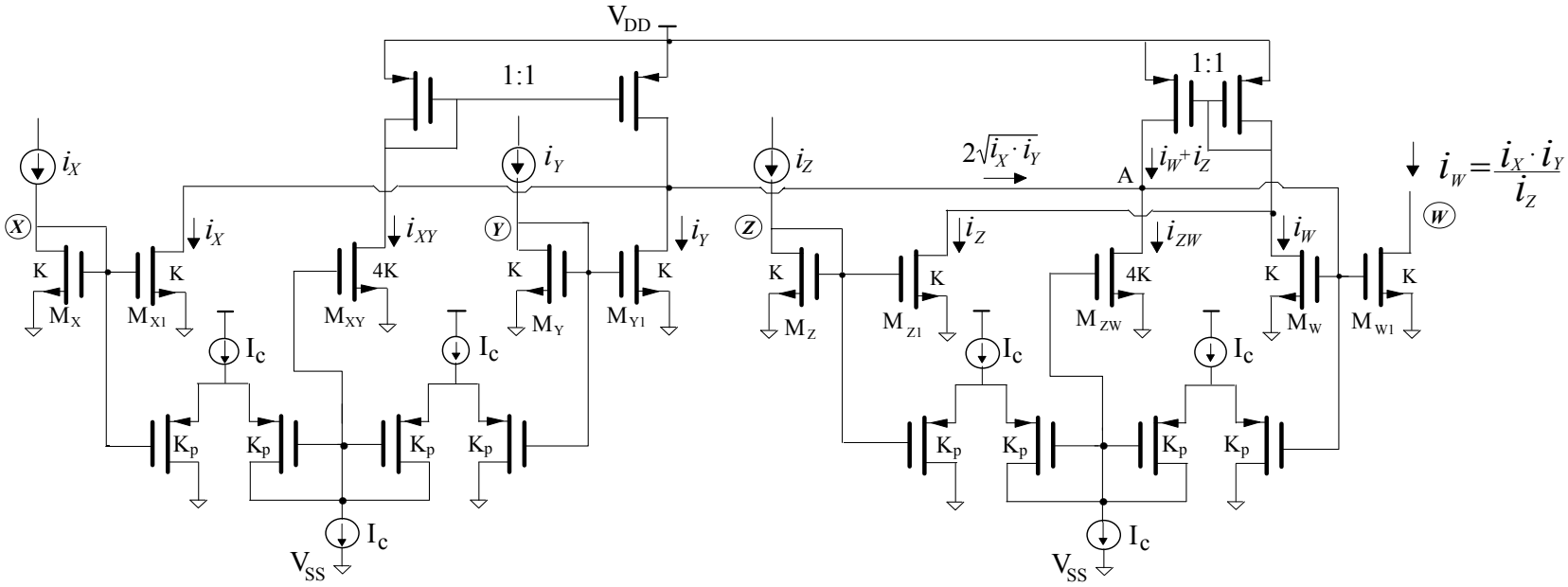


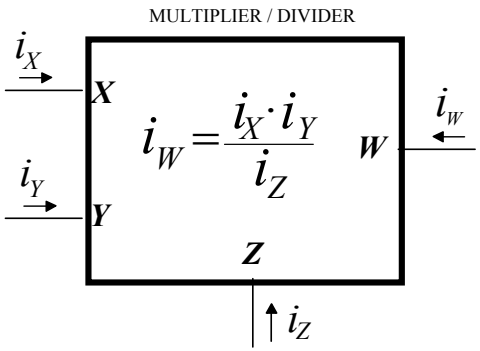
- The voltage averaging subcircuit produces a gate voltage $\upsilon_{X'Y}$, which is forced to be equal with the average of the gate voltages of MX, and MY.

MOS translinear principle: $$\sqrt{i_{XY}} = \sqrt{i_X} + \sqrt{i_Y}$$

Output current: $$i_z = 2\sqrt{i_X . i_Y}$$

Current multiplier topology

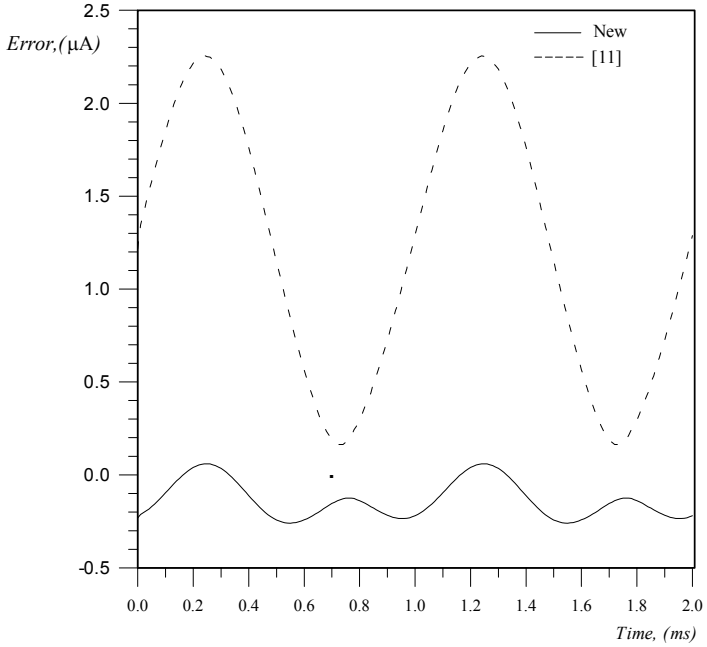


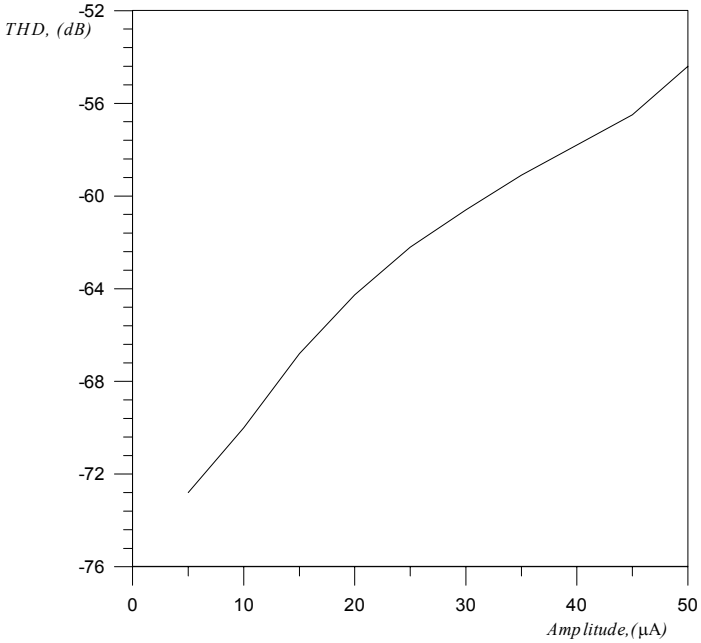


✓It is constructed by two properly connected geometric-mean circuits.

Performance of the proposed multiplier.

•Comparison with a multiplier based on up-down topology.





☺ A reduction of about 50% for the required transistor area is achieved in the proposed circuit.

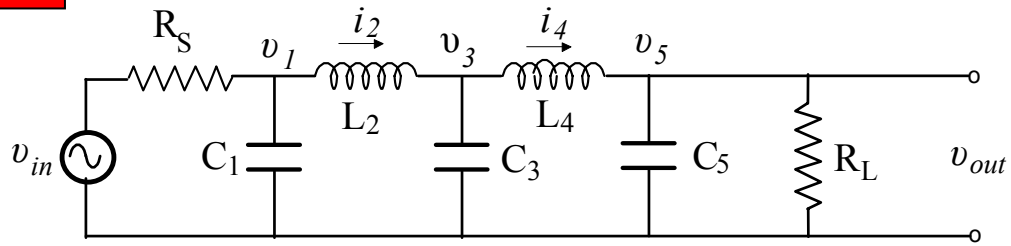
☺The minimum supply voltage requirement for both proposed circuits is:

$$V_{DD\min} = 2V_{DS,SAT} + V_{GS}$$

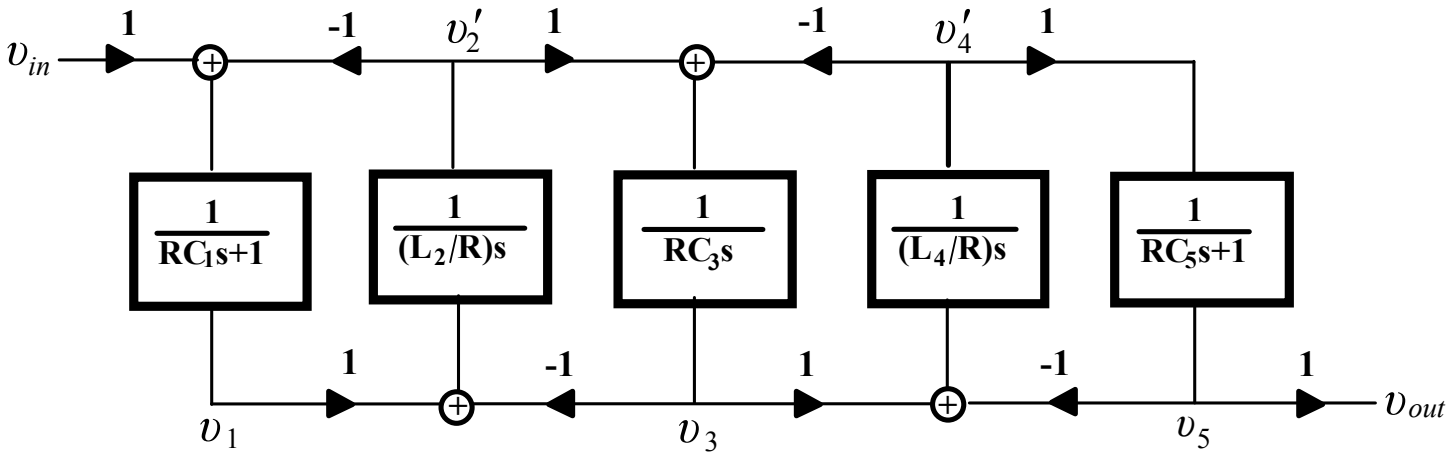
High-order Square-Root-Domain filters

Operational simulation of all-pole LC ladders

✓ **LC ladder prototype**

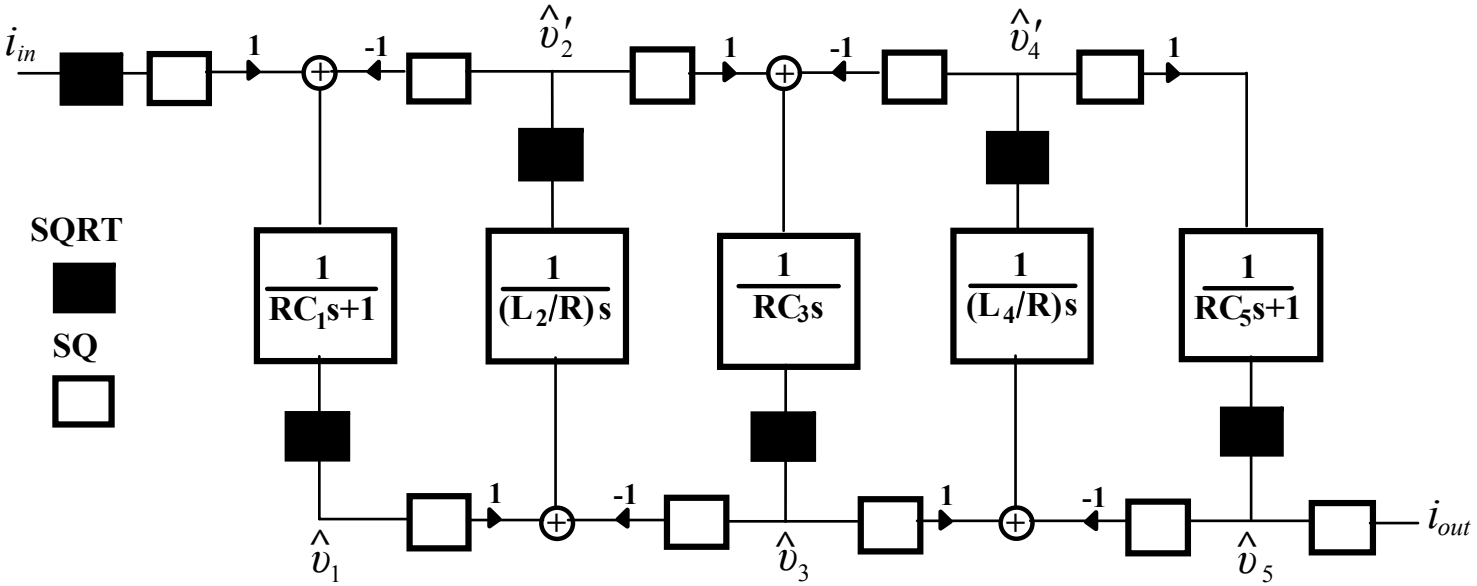


✓ **Linear domain Signal Flow Graph (SFG)**

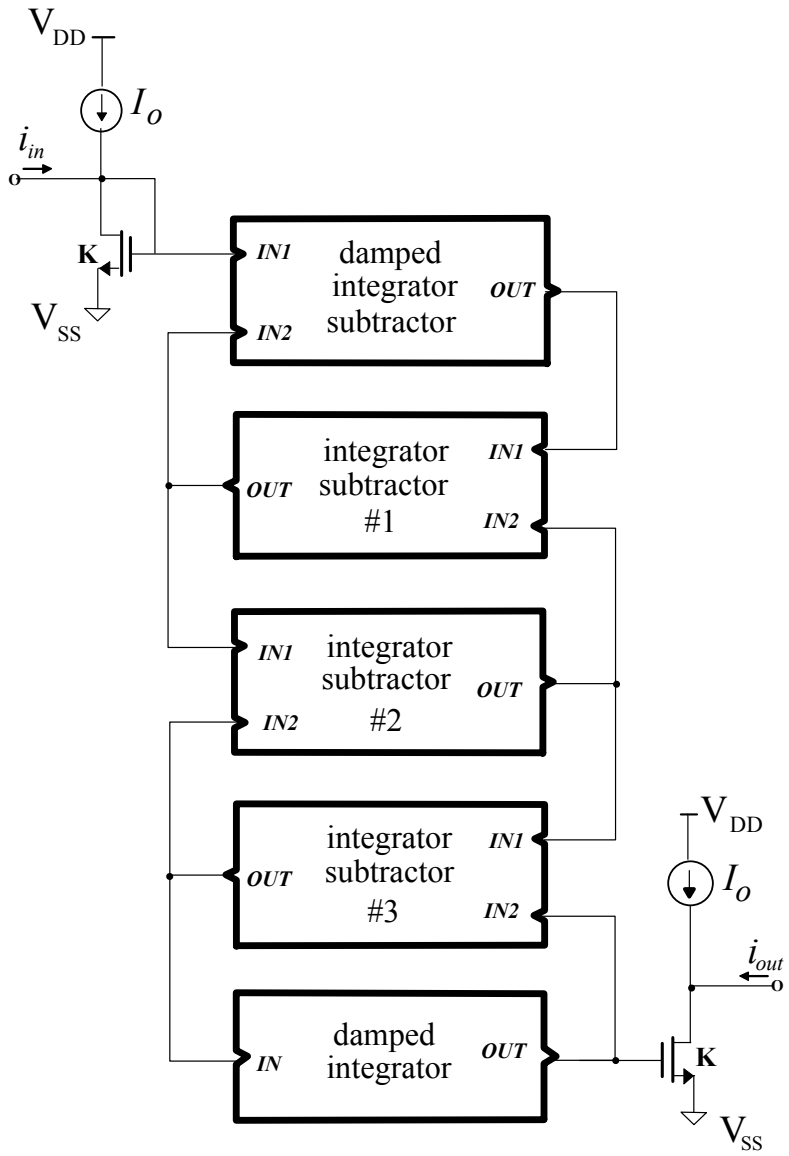


✓ Transposition to Square-Root Domain using the following rules:

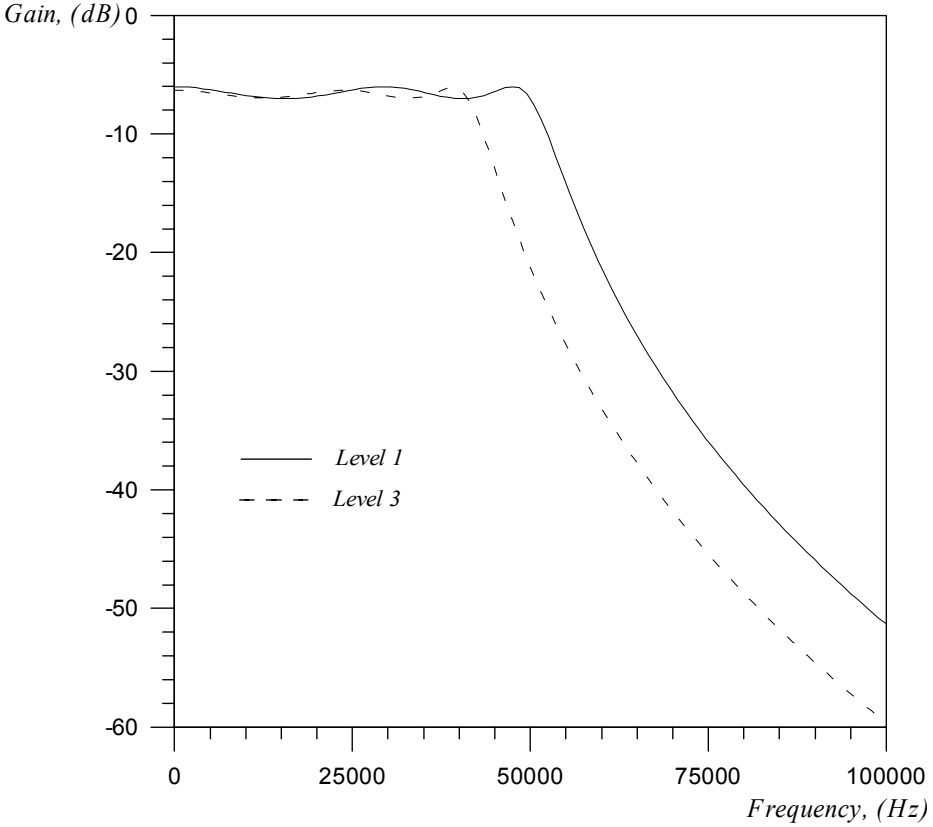
- A SQRT block is placed at the output of each integrator.
- A SQ block is placed at each input of integrators (before scaling).
- A SQRT block is placed at the input of the system.
- A SQ block is placed at the output of the system.

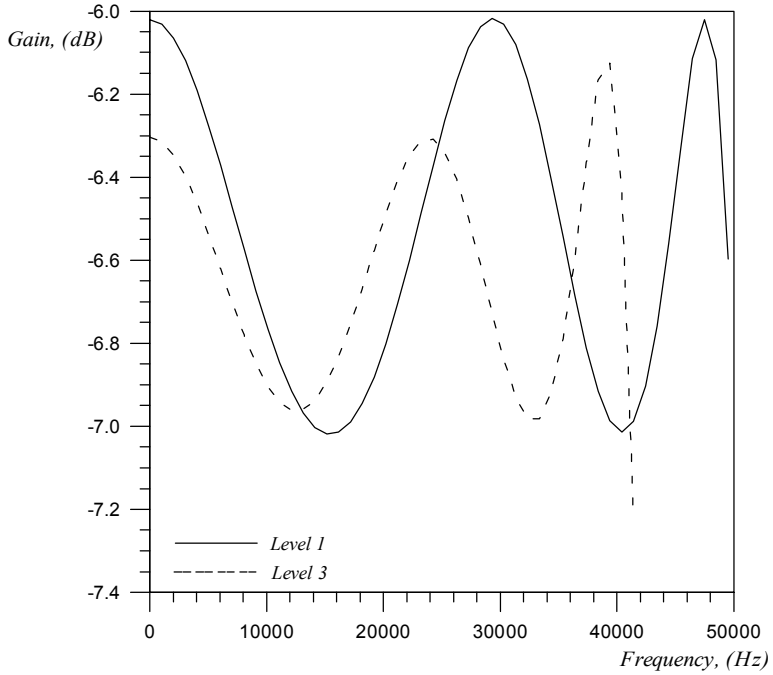


✓ Implementation using Square-Root-Domain cells



Frequency response of the filter @ modulation index factor 0.8

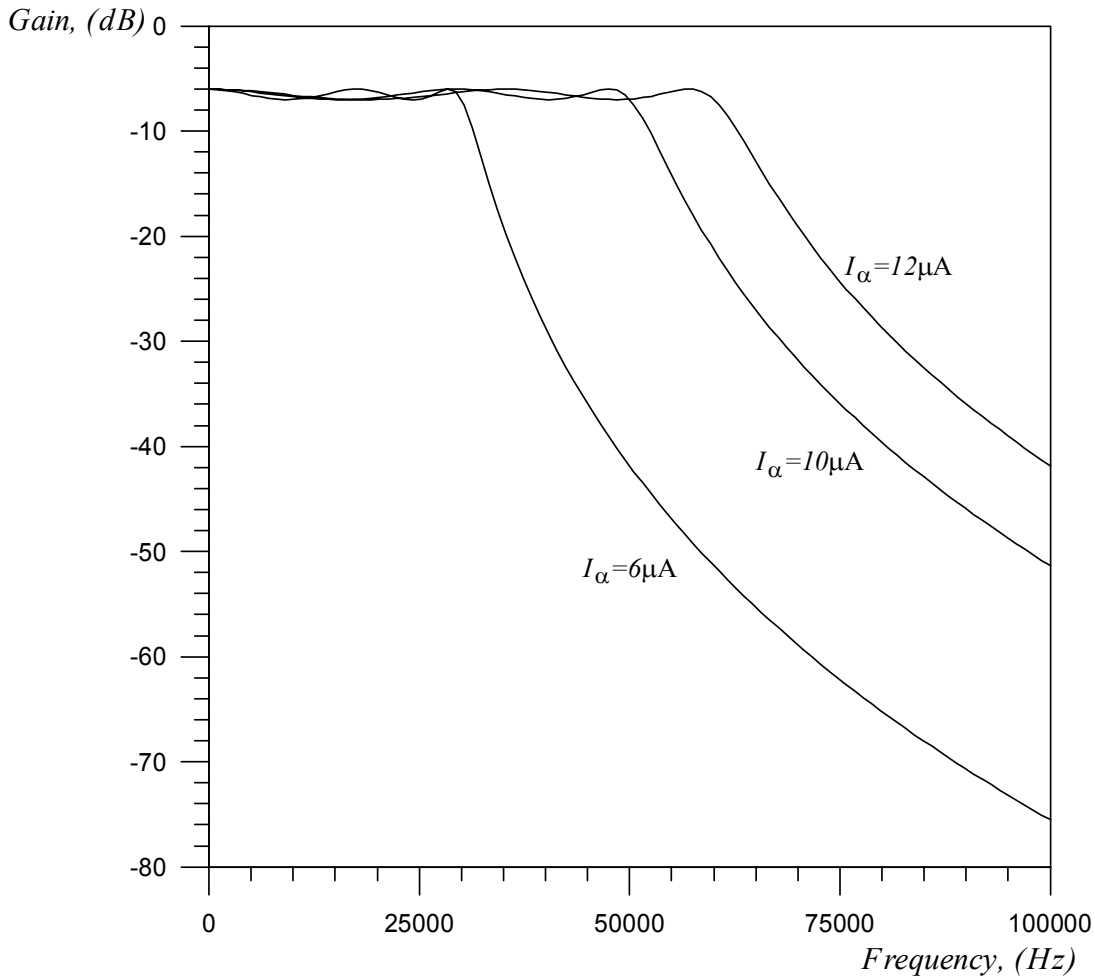




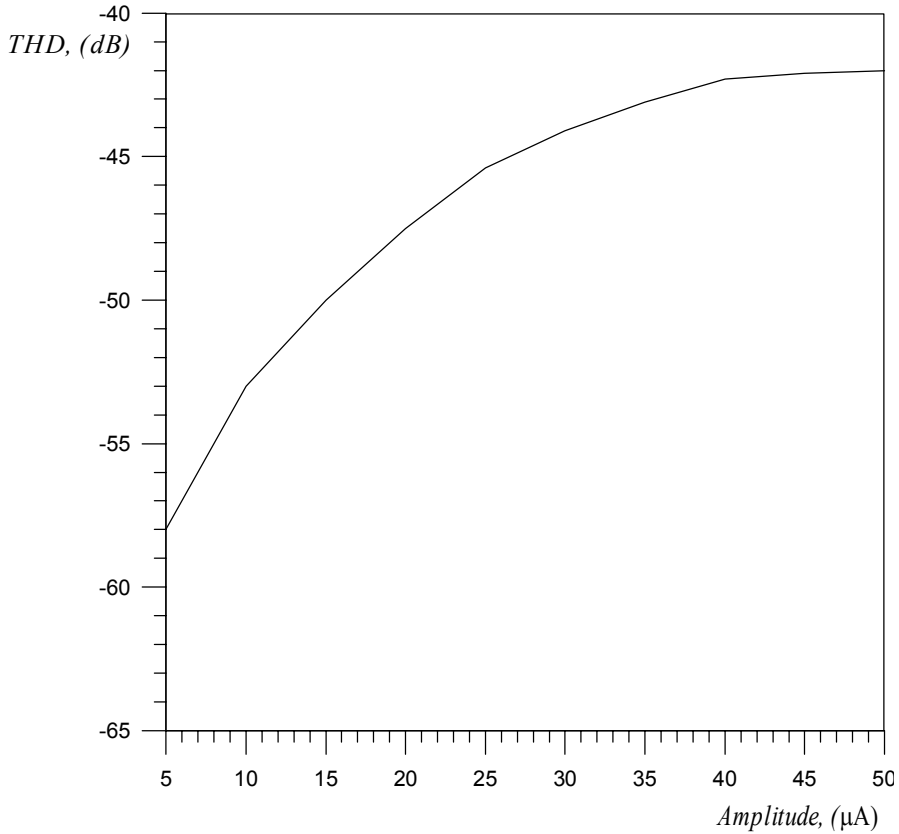
☑ The frequency response of a Square-Root-Domain filter is evaluated using large-signal transient simulations and FFT analysis.

☹ The AC analysis of HSPICE is valid only for small modulation index factor !!!

✓Electronic tuneability of Square-Root-Domain filters.



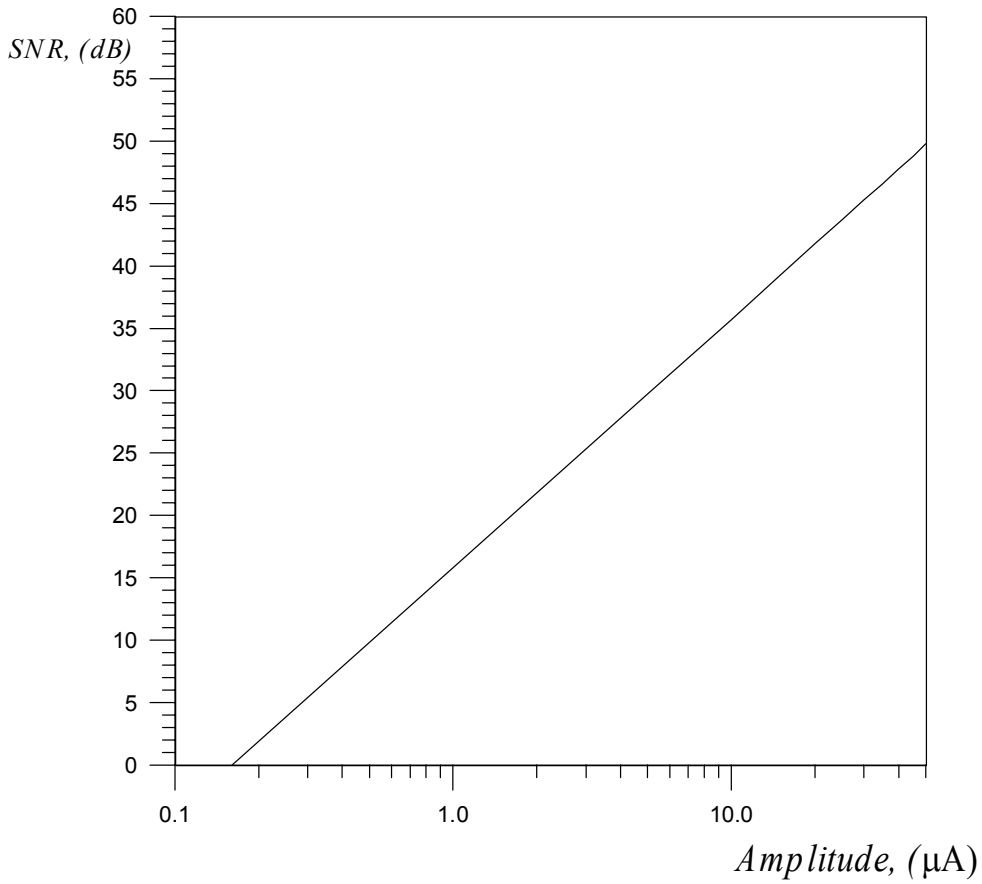
Non-linear analysis



☑ A two-tone test was performed, in order to measure the third-order intermodulation distortion factor.

☺ The IMD3 was -42dB @ modulation index factor equal to 1.

Noise analysis



☺ The achieved Dynamic Range was 49.7dB.

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Square-RootDomain

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